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Generalized DC-Link Voltage Balancing Control Method for Multilevel Inverters

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***Abstract*— This paper presents a general dc-link voltage balancing control method for multilevel inverters based on a generalized space vector pulse width modulation (SVPWM) scheme, with no requirements for additional auxiliary-power circuits. The SVPWM scheme generates all the available switching states and switching sequences based on two simple mappings, and calculates the duty cycles simply as for a two-level SVPWM, thus independent of the level of the inverter. The optimal switching sequence and optimal duty cycles for dc-link voltage balancing control are provided in the paper. Because all the measured signals are instantaneous values, the dc-link voltage balancing control method in the paper is suitable for any load without any assumption on the output current waveforms. The dc-link voltage balancing control in the paper is effective even when the capacitances of the dc-link capacitors of the multilevel inverter are not strictly equal or the voltage of the dc source of the multilevel inverter is fluctuating. Simulation results for a five-level inverter are given.**

***Keywords*— Voltage balancing; SVPWM; multilevel inverter**

I. INTRODUCTION

Multilevel inverters are widely used in high-power high-voltage applications due to their advantageous performance compared to two-level inverters, including reduced voltage stress on the power devices, lower harmonics, lower instantaneous rate of voltage change (*dv*/*dt*), and lower common-mode voltage. However, the inherent voltage drift of the dc-link capacitors of the multilevel inverters degrades the performance of these inverters, in terms of higher voltage stress on the power devices, higher harmonics, higher electromagnetic interference, and so on. If the voltage drift of the dc-link capacitors is not limited during the operation of the multilevel inverter, then the unbalances of dc-link capacitor voltages even lead to the collapse of some of these voltages under a wide range of operating conditions.

Several approaches have been introduced to balance the dc-link voltages of multilevel inverters [1]-[7]. One approach [1] is realized by introducing extra circuits, which requires additional power hardware, and increases the cost and complexity of the system. In another approach [2], the dc-link voltage balancing is achieved with the help of another active power circuit in the system, which, however, is not suitable for a stand-alone multilevel inverter.

The third approach is implemented by modifying the switching pattern of the inverter according to a control strategy to balance the dc-link capacitor voltages, which has recently attracted more and more attention because no additional hardware is needed. Space vector pulse width modulation (SVPWM), also called space vector modulation (SVM), is the most attractive modulation strategy for multilevel inverters because SVPWM provides significant flexibility for optimizing switching waveforms, and because SVPWM is well suitable for digital signal processor implementation. One dc-link voltage balancing control method based on virtual-space-vector PWM is introduced in [3]. However, the sum of the three phase currents is required to be zero, which limits the application of the method, and the complexity of the method will increase dramatically with any increase of the inverter level. Some other SVPWM dc-link voltage balancing schemes based on objective function

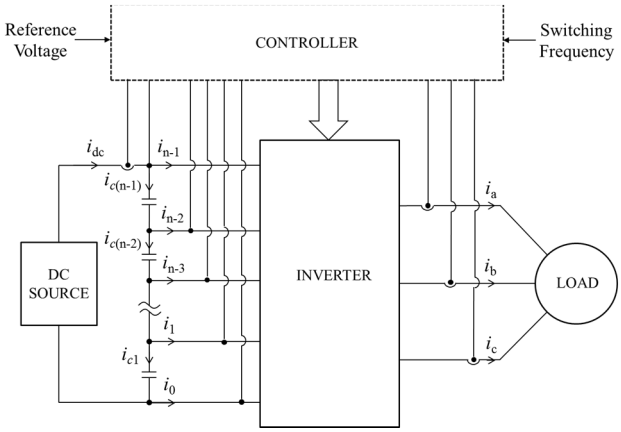


Fig.1. Block diagram of a multilevel inverter

optimization can be found in [4] [5]. In [4] and [5], the sum of the instantaneous currents of the dc-link capacitors are assumed to be zero, which is not accurate when the voltage of the dc source is fluctuating or the capacitances of the dc-link capacitors are not strictly equal. Moreover, the duty cycles of the space vectors are fixed, which cannot provide the best control effect for all operation conditions.

This paper, based on a fast and generalized SVPWM scheme developed in this paper, proposes a new general dc-link voltage balancing method for multilevel inverters, which has the following significant advantages compared with prior approaches: 1) The method provides the optimal switching sequence and the corresponding optimal duty cycles for dc-link voltage balancing; 2) The method is suitable for any load without any assumption on the output current waveforms; 3) No additional auxiliary-power circuits are required; 4) The method is effective even when the dc-link capacitances are not strictly equal or the voltage of the dc source fluctuates; 5) The method is suitable for any level of inverter.

The rest of the paper is organized as follows: Section II describes the SVPWM scheme developed in this paper in detail. Section III proposes the dc-link voltage balancing control. Section IV shows the simulation results for a five-level inverter. Finally, Section V concludes the paper.

II. SVPWM Scheme

For an n-level inverter shown in Fig. 1, the output voltage vector in this paper is defined as

$$\boldsymbol{V}_{out} = (n-1)\cdot(u_a + u_b \cdot e^{j\frac{2}{3}\pi} + u_c \cdot e^{j\frac{4}{3}\pi}) \quad (1)$$

where u_a, u_b, and u_c are the instantaneous output voltages of phases A, B, and C of the inverter, respectively, relative to the negative terminal of the dc source.

When assuming the voltages on the dc-link capacitors are identical, the output voltage vector in (1) becomes

$$\boldsymbol{V}_{out} = V_{dc}\cdot(S_a + S_b \cdot e^{j\frac{2}{3}\pi} + S_c \cdot e^{j\frac{4}{3}\pi}) \quad (2)$$

where V_{dc} is voltage of the DC source, and S_a, S_b, and S_c (S_a, S_b, S_c=0, 1, …n-1) are the switching states of phases A, B, and C, respectively. Accordingly, the voltage of each dc-link capacitor is $V_{dc}/(n-1)$, and the output voltages of phase A, B, and C relative to the negative terminal of the dc source are $S_a\cdot V_{dc}/(n-1)$, $S_b\cdot V_{dc}/(n-1)$, and $S_c\cdot V_{dc}/(n-1)$, respectively. A space vector diagram containing all the output vectors and the corresponding switching states of the inverter can be generated based on (2). For example, Fig. 2 shows the space vector diagram of a five-level inverter calculated in this way, where $\boldsymbol{V}_{ref}$ is the reference vector, and $\boldsymbol{V}_{n1}$, $\boldsymbol{V}_{n2}$, and $\boldsymbol{V}_{n3}$ are the corresponding nearest three vectors. It is the task of the SVPWM scheme to synthesize the reference vector as follows

$$T_s \cdot \boldsymbol{V}_{ref} = d_1 \cdot \boldsymbol{V}_{n1} + d_2 \cdot \boldsymbol{V}_{n2} + d_3 \cdot \boldsymbol{V}_{n3} \quad (3)$$

where T_s is the commanded switching cycle, and d_1, d_2, and d_3 are the duty cycle times of $\boldsymbol{V}_{n1}$, $\boldsymbol{V}_{n2}$, and $\boldsymbol{V}_{n3}$, respectively.

The SVPWM scheme proposed in this paper is briefly shown in Fig. 3. It can generate all the available switching sequences and the corresponding duty cycles according to the

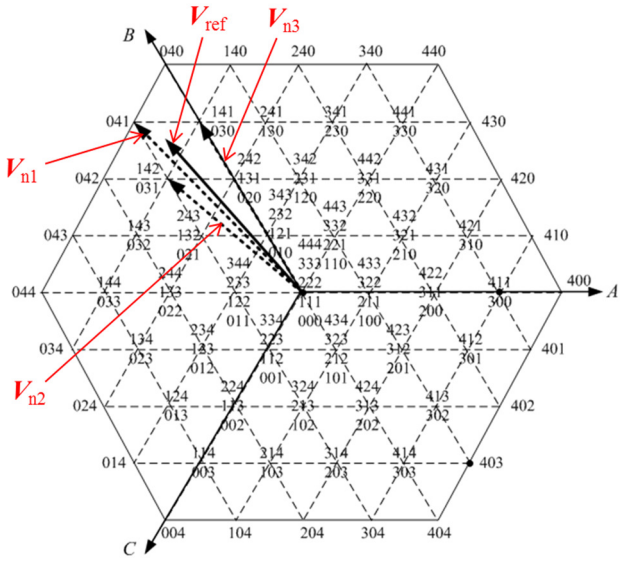


Fig. 2. Space vector diagram of a five-level inverter

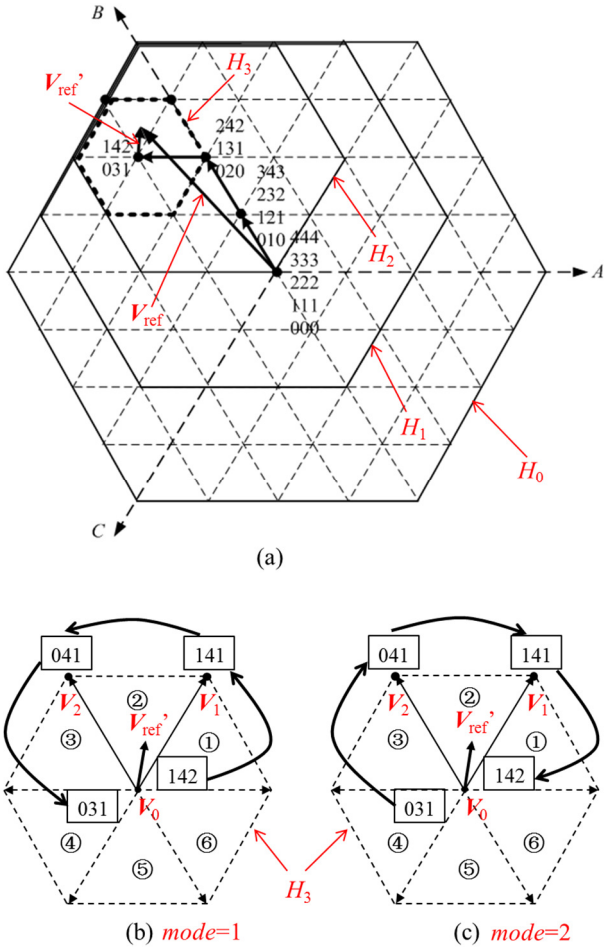


Fig. 3. SVPWM proposed in the paper: (a) Location method for the reference vector; (b)-(c) Two switching sequence modes.

reference voltage and the commanded switching frequency for any level of inverter. For purposes of demonstration, the SVPWM is illustrated based on the space vector diagram of the five-level inverter shown in Fig. 2. The detailed method of generating the switching sequences and calculating the corresponding duty cycles is introduced as follows.

A. *Switching Sequences*

First, the reference vector $\boldsymbol{V}_{\text{ref}}$ is represented as the sum of a set of "vertex vectors" and a "remainder vector" $\boldsymbol{V}_{\text{ref}}'$, as shown in Fig. 3(a). A vertex vector is a vector connecting two adjacent vertices. The vertex vectors connect the center vertex of the n-level space-vector diagram H_0 with a first vertex of the "modulation triangle" (composed by the vertices of the nearest three vectors $\boldsymbol{V}_{\text{n1}}$, $\boldsymbol{V}_{\text{n2}}$, and $\boldsymbol{V}_{\text{n3}}$ as in Fig. 2). The remainder vector is the vector enclosed by the modulation triangle and connecting the first vertex of the modulation triangle with the reference vector.

One way to determine the set of vertex vectors is based on determining a set of nested hexagons H_1, H_2, and H_3 enclosing the reference vector, as shown in Fig. 3(a). Each nested hexagon corresponds to a specific level ranging from (n-1) to a second level, and centers at the vertex of a vertex vector. For instance, the method of selecting the nested (n-1)-level hexagon H_1 is shown in Fig. 4. There are six vertex vectors available for the nested (n-1)-level hexagon H_1, i.e., the one blue solid arrow and five blue dashed arrows as shown in Fig. 4. The actual vertex vector, among the six available vertex vectors, for the nested (n-1)-level hexagon H_1 is the one that the angle between this vertex vector and the reference vector is the smallest. In this way, the first vertex vector can be selected, as the blue solid arrow shown in Fig. 4, and the origin of the reference vector is shifted to the vertex of the selected vertex vector, which is the center vertex of the selected nested hexagon H_1. The other nested hexagons can be selected in a similar way.

Second, based on a function s of the angle φ of the corresponding vertex vector relative to axis A, determine iteratively the switching states at the vertices for each vertex vector in the set of vertex vectors, starting from the present switching states of the inverter at the origin vertex, by modifying (increase or decrease by 1) a corresponding phase of the present switching states to produce the switching states

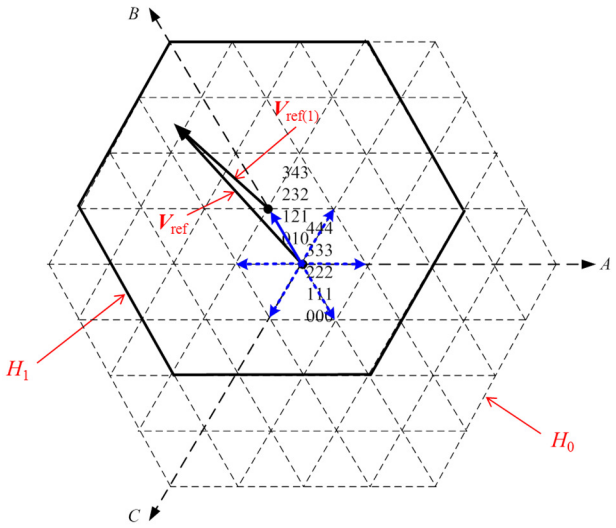


Fig. 4. Selection of the vertex vectors and nested hexagons

of the inverter at the first vertex of the modulation triangle. The function s of the angle φ ($0 \le \varphi < 2\pi$) of the corresponding vertex vector can be described as

$$s = 3\varphi/\pi + 1 \tag{4}$$

The rule of the modification for the switching states and the corresponding phase, called the "first mapping", is shown in Table I, in which the letters A, B, or C means the switching state of phase A, B, or C respectively that needs to be modified. The up-arrow "↑" means the switching state needs to increase by 1, and the down-arrow "↓" means the switching state needs to decrease by 1. Since the switching states for each phase of an n-level inverter can only have a value from 0 to (n-1) by definition in this paper, a modified switching state needs to be excluded when the corresponding switching state of phase A, B, or C is larger than (n-1) or less than 0. Based on the first mapping in Table I, the switching states at the first vertex of the modulation triangle and the vertices of the vertex vectors are shown in Fig. 3(a), which can be verified by comparing it with the space vector diagram of the five-level inverter shown in Fig. 2.

TABLE I. RULE OF THE MODIFICATION OF SWITCHING STATES (FIRST MAPPING)

s	1	2	3	4	5	6
Modification	A↑	C↓	B↑	A↓	C↑	B↓

TABLE II. RULE OF THE DETERMINATION OF SWITCHING SEQUENCES (SECOND MAPPING)

	reg					
	1	2	3	4	5	6
mode=1	ABC↑(L)	CAB↓(U)	BCA↑(L)	ABC↓(U)	CAB↑(L)	BCA↓(U)
mode=2	CBA↓(U)	BAC↑(L)	ACB↓(U)	CBA↑(L)	BAC↓(U)	ACB↑(L)

Finally, based on the switching states obtained at the first vertex of the modulation triangle, determine the switching sequences according to the switching sequence mode (*mode*) and the region number (*reg*) of the modulation triangle in the nested 2-level hexagon H_3 as shown in Fig. 3(b)-(c). There are two switching sequence modes in the paper, i.e., the switching sequence mode is *mode*=1 when the switching sequence is counterclockwise selected as in Fig. 3(b), and the switching sequence mode is *mode*=2 when the switching sequence is clockwise selected as in Fig. 3(c).

The rule of determining the switching sequence, called the "second mapping", is shown in Table II, in which each element of the mapping includes 5 sub-elements. The letter A, B, or C means the switching state of phase A, B, or C is to be modified sequentially. The symbol "↑" or "↓" means the state of the corresponding phase is increased by 1 or decreased by 1, respectively. In the space vector diagram, the redundant switching states at each vertex are listed decreasingly from top to bottom corresponding to the switching states of phase A, as shown in Fig. 2. The letter "L" in the parentheses represents the word "lower" and means the first switching state at the first vertex of the modulation triangle should not be the top one, and the letter "U" in the parentheses represents the word "upper" and means the first switching state at the first vertex of the modulation triangle should not be the bottom one. Based on the second mapping, the switching sequences according to different switching sequence modes are 142 → 141 → 041 → 031 (*mode*=1) and 031 → 041 → 141 → 142 (*mode*=2), as shown in Fig. 3(b)-(c), and the accuracy of the switching sequences can be verified by comparison with the space vector diagram shown in Fig. 2.

When the modulation index of the reference vector is low (the magnitude of the reference vector is relatively small), there will be more than one available switching sequence generated by the SVPWM scheme, which provides significant flexibility to optimize switching patterns. For example, a reference vector $\boldsymbol{V}_{\text{ref}}$, with low modulation index, and the corresponding remainder vector $\boldsymbol{V}_{\text{ref}}$' are shown in Fig. 5.

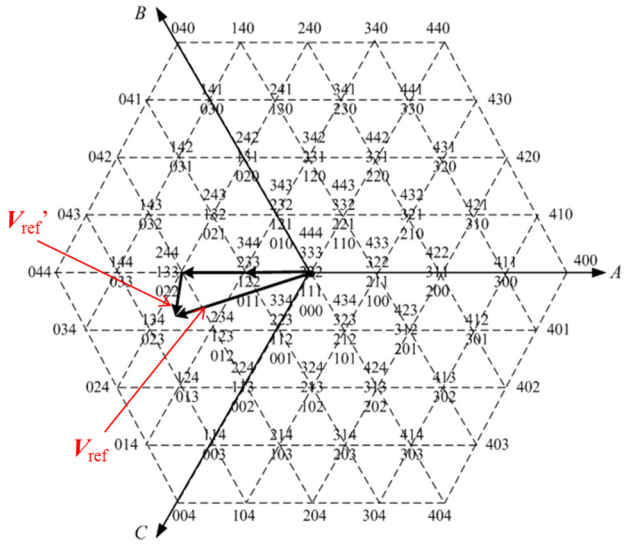


Fig. 5. A reference vector with low modulation index

There are two switching sequences generated by the proposed SVPWM scheme for each switching sequence mode, e.g., 022 → 023 → 123 → 133 and 133 → 134 → 234 → 244 for *mode*=1.

In summary, the first mapping and the second mapping are suitable for any level inverter and any reference vectors with any modulation indexes, and the second mapping can be conveniently extended to meet other specific requirements, e.g., symmetric switching sequences. This will be introduced in further papers.

B. Calculation of the Duty Cycles

Based on the remainder vector $\boldsymbol{V}_{\text{ref}}$', as shown in Fig. 3(b)-(c), the duty cycles of the "nearest three vectors" are determined as for a two-level SVPWM, thus independent of the level of the inverter.

Equation (3) now becomes

$$T_s \cdot \boldsymbol{V}'_{ref} = V_{dc} \cdot (T_1 \cdot e^{j(reg-1)\pi/3} + T_2 \cdot e^{j \cdot reg \cdot \pi/3}) \quad (5)$$

where T_s is the commanded switching cycle; *reg* is the region number of the modulation triangle in the nested 2-level hexagon H_3 as shown in Fig. 3(b)-(c); T_1 and T_2 are the duty cycle times of $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$, respectively.

Finally, the duty cycles, as shown in Fig. 6, are obtained as follows

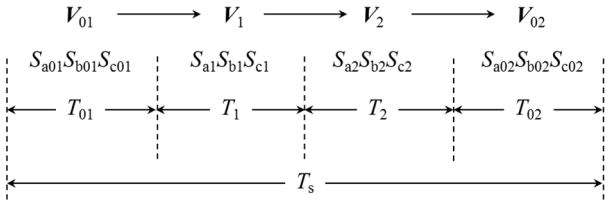


Fig. 6. Switching sequence and duty cycles

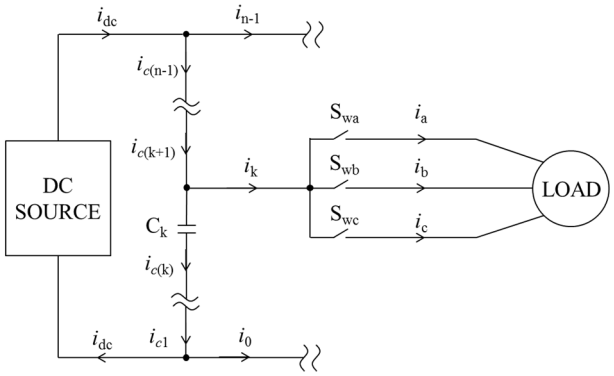


Fig. 7. Currents for an *n*-level inverter

$$\begin{cases} T_1 = \frac{2}{\sqrt{3}}\left[V_{rx}\, sin\left(\frac{reg}{3}\pi\right) - V_{ry}\, cos\left(\frac{reg}{3}\pi\right)\right]\cdot T_s \\ T_2 = -\frac{2}{\sqrt{3}}\left[V_{rx}\, sin\left(\frac{reg-1}{3}\pi\right) - V_{ry}\, cos\left(\frac{reg-1}{3}\pi\right)\right]\cdot T_s \\ T_0 = T_s - T_1 - T_2 \end{cases} \tag{6}$$

where V_{rx} and V_{ry} represent the real and imaginary part of $\boldsymbol{V}_{ref}'/V_{dc}$, respectively; T_0 is the total duty cycle for the vectors from the center vertex of the n-level hexagon H_0 to the center vertex of the nested 2-level hexagon H_3, or called the "zero vectors" in this paper.

In the proposed new SVPWM scheme, two switching states at the center vertex of the nested 2-level hexagon are used, and each switching state represents a "zero vector". The duty cycles T_{01} and T_{02} of the two zero vectors can be freely adjusted as long as the following equation is met

$$T_{02} = T_0 - T_{01}, \quad 0 \le T_{01} \le T_0 \tag{7}$$

In summary, based on the proposed new SVPWM scheme, both the switching sequence and the duty cycles of the zero vectors can be adjusted to control the dc-link capacitor voltages, which will be introduced in the next section in detail.

III. DC-Link Voltage Balancing Control

Fig. 7 shows the relationship between the currents of the multilevel inverter in Fig. 1. The voltages across the dc-link capacitors (at a sampling time t_0) from bottom to top are named as v_1, v_2, …v_{n-1}, and the expected voltage, i.e., the voltage after a switching cycle T_s, across the k^{th} capacitor C_k (k=1, 2, …n-1), is

$$v_k' = v_k + \bar{i}_{c(k)} \cdot T_s / C_k \tag{8}$$

where $\bar{i}_{c(k)}$ is the average value of $i_{c(k)}$ (the instantaneous current of capacitor C_k) during one switching cycle, and is given by

$$\bar{i}_{c(k)} = \frac{1}{T_s}\int_{t_0}^{t_0+T_s} i_{c(k)}\, dt \tag{9}$$

Equations (8) and (9) reveal that the voltages of the dc-link capacitors can be controlled by controlling their currents.

The currents of the dc-link capacitors are determined by the input currents i_0, i_1, i_2, …i_{n-1} of the inverter and the output current i_{dc} of the dc source, as shown in Fig. 1 and Fig. 7. The relationship is

$$i_{c1} = i_0 + i_{dc} \tag{10}$$

and

$$i_{c(k+1)} = i_{c(k)} + i_k \tag{11}$$

where k=1, 2, …n-2. Equations (10) and (11) yield the current of capacitor C_k (k=1, 2, …n-1) as

$$i_{c(k)} = \sum_{m=0}^{k-1} i_m + i_{dc} \tag{12}$$

As shown in Fig. 7 (the equivalent "switches" S_{wa}, S_{wb}, and S_{wc} are closed only if the switching states of phases A, B, and C are equal to k, respectively), the currents i_0, i_1, i_2, …i_{n-1} are determined by the output currents i_a, i_b, and i_c and the switching states of the inverter as [6]

$$i_k = \delta(S_a - k)\cdot i_a + \delta(S_b - k)\cdot i_b + \delta(S_c - k)\cdot i_c \tag{13}$$

where k=0, 1, 2, …n-1, and $\delta(\neq 0)$=0, $\delta(0)$=1.

Assuming i_a, i_b, and i_c are constant during a switching cycle, the average values of the currents i_0, i_1, i_2, …i_{n-1} according to the switching sequence in Fig. 6 are obtained from (9), (12) and (13) as

$$\begin{aligned} \bar{i}_k = \frac{1}{T_s}\{ & \\ & [\delta(S_{a01}-k)i_a + \delta(S_{b01}-k)i_b + \delta(S_{c01}-k)i_c]\cdot T_{01} \\ & +[\delta(S_{a1}-k)i_a + \delta(S_{b1}-k)i_b + \delta(S_{c1}-k)i_c]\cdot T_1 \\ & +[\delta(S_{a2}-k)i_a + \delta(S_{b2}-k)i_b + \delta(S_{c2}-k)i_c]\cdot T_2 \\ & +[\delta(S_{a02}-k)i_a + \delta(S_{b02}-k)i_b + \delta(S_{c02}-k)i_c]\cdot T_{02}\} \\ & = \beta_{1(k)}\cdot T_{01} + \beta_{2(k)} \end{aligned} \tag{14}$$

where k=0, 1, 2, …n-1, and $\beta_{1(k)}$ and $\beta_{2(k)}$ are constants according to a certain switching sequence, and defined by

$$\begin{cases} \beta_{1(k)} = \frac{1}{T_s}\{[\delta(S_{a01}-k) - \delta(S_{a02}-k)]\cdot i_a \\ \quad +[\delta(S_{b01}-k) - \delta(S_{b02}-k)]\cdot i_b \\ \quad +[\delta(S_{c01}-k) - \delta(S_{c02}-k)]\cdot i_c\} \\ \beta_{2(k)} = \frac{1}{T_s}\{[\delta(S_{a1}-k)i_a + \delta(S_{b1}-k)i_b + \delta(S_{c1}-k)i_c]T_1 \\ \quad +[\delta(S_{a2}-k)i_a + \delta(S_{b2}-k)i_b + \delta(S_{c2}-k)i_c]T_2 \\ \quad +[\delta(S_{a02}-k)i_a + \delta(S_{b02}-k)i_b + \delta(S_{c02}-k)i_c]T_0\} \end{cases} \tag{15}$$

Substituting (14) and (12) into (8), yields the voltage of the k^{th} capacitor C_k (k=1, 2, …n-1) after a switching cycle as

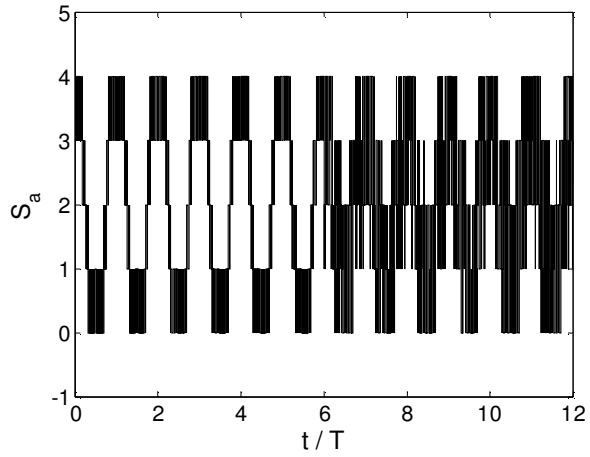
$$v_k' = \alpha_{1(k)}\cdot T_{01} + \alpha_{2(k)} \tag{16}$$

where $\alpha_{1(k)}$ and $\alpha_{2(k)}$ are constants, and

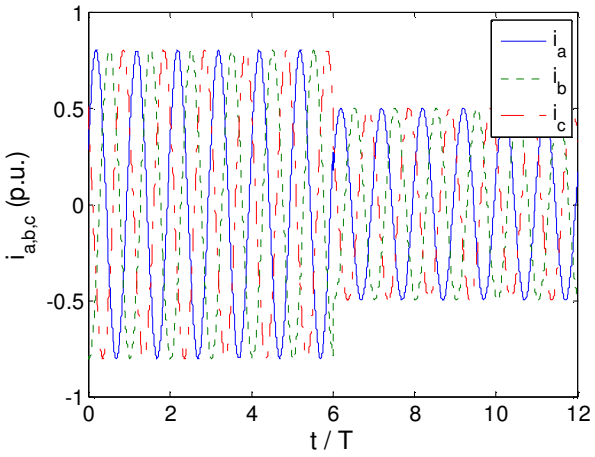
$$\begin{cases} \alpha_{1(k)} = \frac{T_s}{C_k}\sum_{m=0}^{k-1}\beta_{1(m)} \\ \alpha_{2(k)} = v_k + \frac{T_s}{C_k}\sum_{m=0}^{k-1}\beta_{2(m)} + \frac{T_s}{C_k} i_{dc} \end{cases} \tag{17}$$

The dc-link voltage balancing control can be achieved by minimizing the following objective function J representing the variation of the voltages across the dc-link capacitors

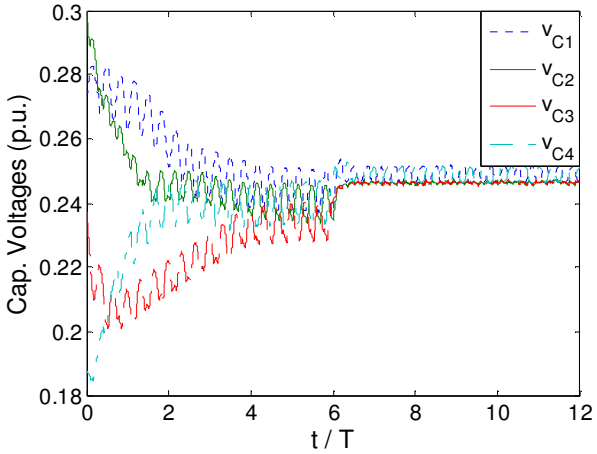
$$J = \sum_{k=1}^{n-1}\sigma_k\left(v_k' - \frac{V_{dc}}{n-1}\right)^2 \tag{18}$$



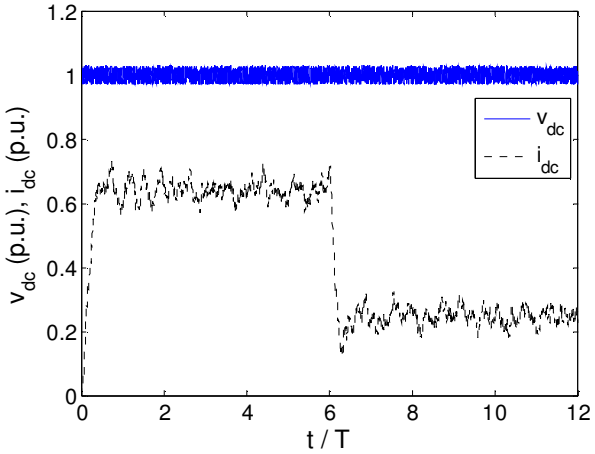
(a) Switching state of phase A



(b) Three-phase output currents of the inverter



(c) Voltages of the capacitors



(d) Voltage and output current of the dc source

Fig. 8. Simulation results: power factor *PF*=0.35; modulation index *m*=0.8 (*t*/*T*<6) and *m*=0.5 (*t*/*T*>6)

where σ_k>0 (k=1, 2, …n-1) is a weighting factor, which is taken into consideration for the case that the capacitances of the dc-link capacitors are not strictly equal, and can be selected as σ_k=1 if all the dc-link capacitors are identical. The purpose of minimizing the objective function J in (18) is to force the voltages across the dc-link capacitors to be as close as possible to the desired value, i.e., $V_{dc}/(n\text{-}1)$.

For a certain switching sequence as in Fig. 6, the value of v_k' is determined by T_{01} as in (16), and the optimal T_{01}, which makes the derivative of J to be zero (dJ/dT_{01}=0) and thus minimizes the objective function J, can be obtained as

$$T_{opt} = -\frac{\sum_{k=1}^{n-1}\sigma_k\left(\alpha_{2(k)}-\frac{V_{dc}}{n-1}\right)\alpha_{1(k)}}{\sum_{k=1}^{n-1}\sigma_k\alpha_{1(k)}^2} \tag{19}$$

Considering a feasible value of T_{01} is required to be 0≤ T_{01}≤ T_0, the optimal T_{01} according to the certain switching sequence as in Fig. 6 is

$$T_{01} = \begin{cases} T_{opt}, & if\ (0 \le T_{opt} \le T_0); \\ 0, & if\ (T_{opt} < 0); \\ T_0, & if\ (T_{opt} > T_0). \end{cases} \tag{20}$$

When the modulation index of the reference vector is low, as shown in Fig. 5 for example, there will be more than one switching sequence available for each switching sequence mode. The optimal T_{01} and the corresponding J for each switching sequence can be calculated by (20) and (18), and finally the optimal switching sequence is the one producing the smallest J.

IV. Results

Finally, simulation results for a five-level inverter are shown in Fig. 8.

In the simulation, a 5% fluctuation is added to the dc source, as shown in Fig. 8(d); the initial voltages across the dc-link capacitors are intentionally non-identical as $1.1V_{dc}/4$, $1.2V_{dc}/4$, $0.95V_{dc}/4$, and $0.75V_{dc}/4$, as shown in Fig. 8(c); the dc-link capacitors are 1.05pu, 1.02pu, 0.98pu, and 0.95pu (the

weighting factors in (18) are all selected to be 1); the power factor of the load is *PF*=0.35; and the modulation index of the reference vector is 0.8 and 0.5 respectively for the first half and the latter half of the time.

Based on the proposed dc-link voltage balancing control method, the voltages across the dc-link capacitors are shown in Fig. 8(c), which reveals that the voltages across the dc-link capacitors are driven to the desired value for both the first half and the latter half of the time, even when the dc-link capacitances are not identical and the voltage of the dc source is fluctuating.

Fig. 8(c) also shows that the proposed dc-link voltage balancing control is more effective when the modulation index of reference voltage is lower (modulation index *m*=0.5) than that when the modulation index of reference voltage is higher (modulation index *m*=0.8). The reason is that when the modulation index of reference voltage is low, there will be more available switching sequences for selection, as shown in Fig. 5, which provide more flexibility for optimizing the switching patterns.

V. CONCLUSIONS

This paper proposes a new general dc-link voltage balancing control method for multilevel inverters, which has the following significant advantages: 1) The method provides the optimal switching sequence and the corresponding optimal duty cycles for dc-link voltage balancing; 2) The method is suitable for any load without any assumption on the output current waveforms; 3) No additional auxiliary-power circuits are required; 4) The method is effective even when the dc-link capacitances are not identical or the voltage of the dc source is fluctuating; 5) The method is suitable for any level of inverter.

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