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A 5-Level Discrete-Time Power Encoder with Measured Coding Efficiency of 70% for 20-MHz LTE Digital Transmitter

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Abstract — This paper reports the recent development on power coding method of generating a 5-level intermediate frequency PWM-based high speed digital-RF bit train, which is used as the input switching signal for class-S digital RF power amplifiers in the digital transmitter. By introducing the discrete-time power coding process at an IF of around 60 MHz, digital transmitter at cellular bands then becomes feasible to implement with current FPGA technologies. It can lower the required sampling rate more than 10 times compared with RF carrier PWM. In addition, a linearizer is designed using a look-up-table to minimize the nonlinear coding effects of the power encoder. The demonstrator shows the state-of-the-art measured power coding efficiency of 70.47% and SNR>30dB for a 20 MHz LTE signals with PAPR of 10.25 dB at 1.9 GHz with our proposed approach.

Index Terms — Digital transmitter, software defined radio, switch mode power amplifier, coding efficiency, gallium nitride, pulse width modulation, FPGA

I. Introduction

The digital transmitter (TX) technology is under rapid development to address the ever increasing complicated radio challenges in LTE and future 5G mobile communications. Its flexible re-configurability is the most attractive feature for software defined radio [1]. With the further development of GaN HEMT technologies, advanced switch-mode RF power amplifiers (PA), such as class-S, have demonstrated very promising potential at cellular bands for digital transmitter [2]. Because of its quite different operation principles from traditional switch-mode PA (e.g. class-E, -F), regardless of signal PAPR, the class-S digital PA is able to efficient amplify constant amplitude high speed digital-RF bit train at several Gbps (generated by power encoder unit) with good linearity at switching stage [3]. Nevertheless, there are still numerous challenges for performance enhancement on class-S PA based TX, such as drivers, reconstruction filter, switching transistor, and power encoder. Among them, power coding plays a central role, since it can alleviate the stringent requirements on the other mentioned aspects. More importantly, coding efficiency and distortion of encoder will have significant impact on the digital TX efficiency and linearity [4].

To date, delta-sigma modulator is the main coding technique for class-S PA in publications, with the key advantages of very good signal to noise ratio. However, it normally has very low power coding efficiency (below 20%) for modulated signals, caused by large amount of out-of-band noise from quantization and noise-shaping thus limiting the switch-mode PA and overall TX efficiency [5]. Another approach is pulse width modulation (PWM) with higher power coding efficiency [6]. However, to perform PWM at cellular bands would require extremely high sampling speed (>20x RF carrier frequencies) for accurate oversampling. Although this can be done using specially designed PWM modulator RFIC operating in continuous-time (analog) domain, it is not suitable for all-digital transmitter applications because of the inflexibility.

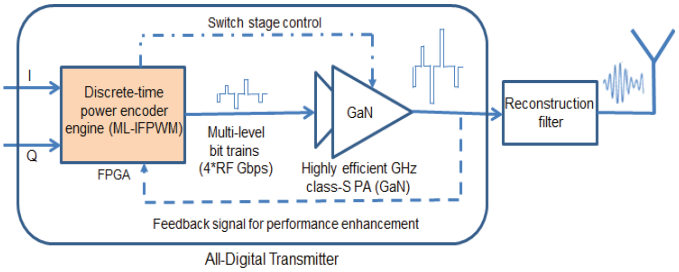


Fig. 1. All-digital transmitter architecture based on multi-level PWM power coding and highly efficient class-S digital PA.

Thus, there is indeed a strong need to develop a new power coding approach in discrete-time (digital) domain with both high coding efficiency, acceptable SNR, and feasibility for practical implementation using digital signal processor such as FPGA (field programmable gate array). To truly enable efficient operation of class-S switch-mode PA in digital TX, we propose a new power coding concept as shown in Fig. 1: multi-level intermediate frequency pulse width modulation (ML-IFPWM) power coding. For the first time, we demonstrated its practical feasibility using a commercial FPGA chip for a 20-MHz LTE signal at RF carrier frequency around 1.9 GHz with state-of-the power coding efficiency. The power coding concept and features are described in section II. Design and practical FPGA implementation for a 5-level demonstrator with measured results are given in section III.

II. Power Coding Approach

In this work, we propose to perform the discrete-time PWM based power coding in two stages, as shown in Fig. 2.

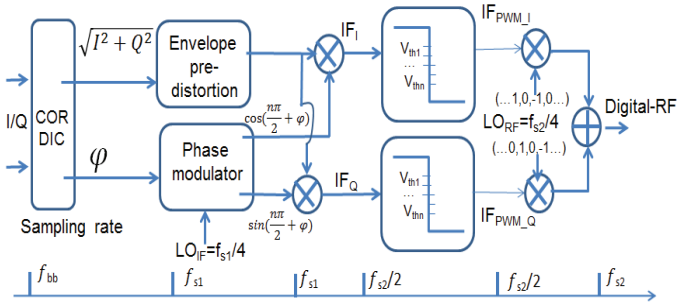


Fig. 2. Multi-level discrete-time IFPWM power coding diagram.

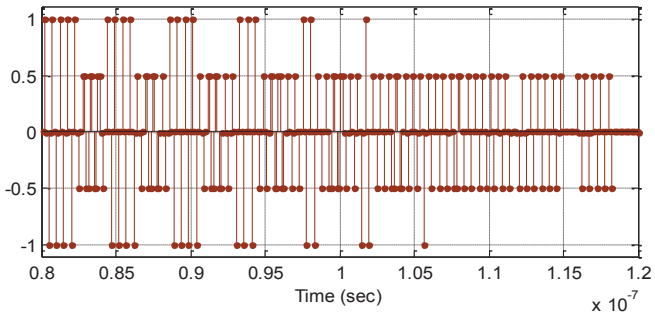


Fig. 3. Simulated 5-level discrete-time digital-RF out of encoder.

Baseband input I/Q signals are firstly converted to an intermediate frequency (IF) with a digital oscillator LOIF (e.g. 61.44 MHz, depending on the signal bandwidth, PAPR, details provided in section III). After that, fixed threshold based pulse width modulation is performed with respect to the pre-distorted IFI and IFQ with a high sampling frequency at half of fs2, providing a high over sampling ratio (e.g. OSR: 32).

This significantly lowers the sampling frequency requirement compared with RF PWM to have the same OSR. In the second stage, the generated IF_{PWM_I} and IF_{PWM_Q} are up-converted to the RF carrier frequency with another four-phase digital LO_{RF}. Finally, they are interleaved to produce the multi-level digital-RF switching signal.

The key features of our approach are summarized as follows:

1). The envelope pre-distortion minimizes the nonlinear transform of PWM. The derived AM-AM transfer function of the multi-level quantizer is:

$$f(a(t)) = \frac{1}{N}\sum_{i=1}^{N}\cos\left[\sin^{-1}\left(\frac{V_{thi}}{a(t)}\right)\right]$$

where a(t) is the envelope, and V_{thi} is the i^{th} threshold, $V_{thi}<V_{thj}$, when $1 \le i \le j \le N$. The inverse function is numerically solved by building a look-up table mapping. This applies in particular for quantization level greater than 3, where the analytical inverse function is very complicated or not possible to derive. Also, it is efficient to be implemented using digital signal processor.

2). Our simulation results have shown that threshold levels in multi-level PWM affects the final power coding efficiency. Thus, determination and further optimization of these quantization reference levels are necessary, which are in general dependent on the signal profile. The details of this part will be reported in future publications.

It is known that power coding efficiency will increase with increasing the quantization level. The proposed multi-level PWM solutions address well the challenges mentioned above. The higher number of quantization levels, the better coding efficiency of the encoder in theory. However, considering the practical control complexity of switch devices, 5-level is a good compromise between performance and complexity. Agilent SystemVue and Matlab co-simulation is performed to develop the power coding scheme with real LTE signals.

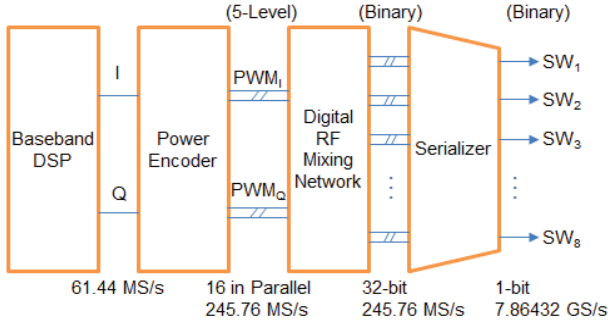


Fig. 4. All-Digital transmitter FPGA implementation for generating the switching signal for multi-level class-S digital PA.

Simulated coding efficiency of a 20 MHz LTE signal of 10.25dB PAPR using 5-level PWM is 75% with SNR of 30dB, with Fig. 3 showing the simulated output Digital-RF bit trains.

III. Implementation and Measurement

Currently, published papers mainly use CW signal or square wave and offline demonstration measurement with high speed arbitrary wave generator (AWG) to evaluate the power coding performance of developed algorithm. This is still far from the digital transmitter operation in practice. Here, we implement the developed coding algorithm using FPGA to real-time process 20 MHz LTE signal at 1.9 GHz RF carrier frequency.

A brief architecture of the FPGA implementation of 5-level IF PWM is shown in Fig. 4. High output sampling rate is essential to faithfully quantize the IF signals and to generate Gbps digital-RF signals. In order to achieve such high throughput, we employ a heavily parallelized architecture. A carefully designed polyphase interpolation filters forwards the identical inputs to the 16 paralleled unites, thus each maintaining low sampling rate. After encoding the IF signals, FPGA GTX (Gigabit Transceiver) sequentially transmits the parallel to serial converted digital bits. We used Xilinx VC707 as development board. 20 MHz LTE baseband signal (from SystemVue) has a sample rate of 61.44 Msps (f_{bb}). Considering the FPGA system clock limitation and practical design complexity (<300MHz), f_{s1} has been chosen to be four times of f_{bb}. The final stage sample rate is 7864.21 Msps,

which is the final data rate of the serial digital-RF bit train (f_{s2}).

Considering the extended class-S H bridge topology as shown in Fig. 5, for 5-level class-S PA operation, eight GaN switching transistors will be needed with each in binary status (ON/OFF). Thus, in the FPGA design, a mapper unit is needed to control the individual transistor using SW1~SW8 switch signal properly. A wideband driver stage is needed for amplifying the FPGA output to completely turn on and pinch off GaN switching HEMT. Normally, a bandpass filter is used to reconstruct the analog RF signal for antenna radiation.

To evaluate the power coding efficiency of the implemented algorithm, a 4-way wideband power combiner (Mini-Circuits: ZN4PD1-50-S+, 500-MHz~5-GHz) is used to combine the multiple SMA outputs from FPGA GTX ports via FMC extension boards, which equivalent represents the 5-level Digital-RF signal in Fig. 5. The bandwidth of the combiner needs to at least cover the side bands of PWM spectrum. Fig. 6 shows the experimental setup for characterizing the FPGA implemented encoder performance.

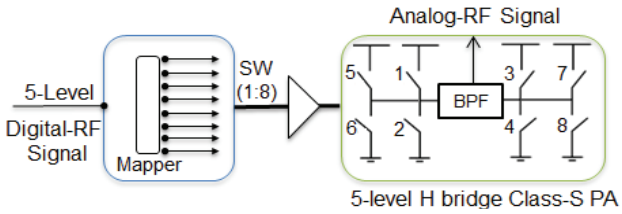


Fig. 5. FPGA control and topology of 5-level class-S PA.

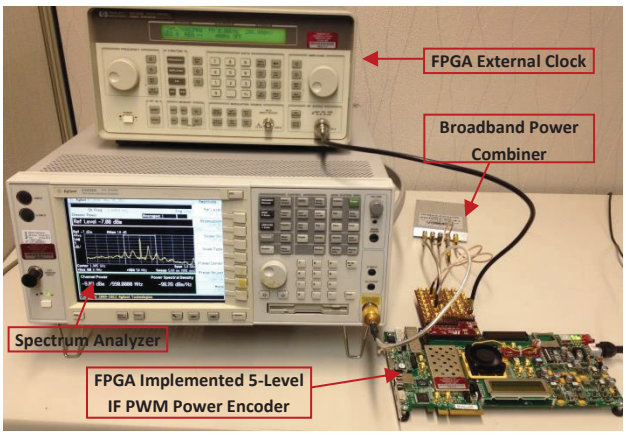
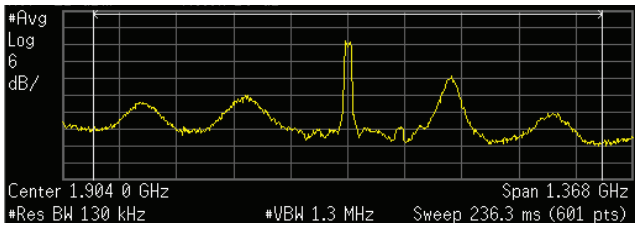


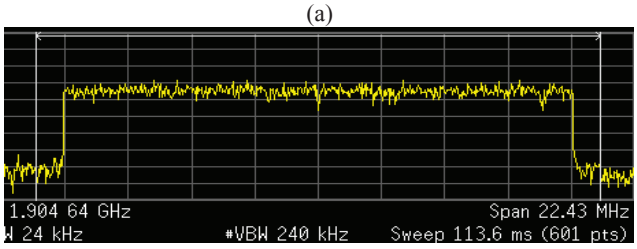
Fig. 6. Test bench for measuring the spectrum of FPGA implemented power encoder generated 5-level switching signals.

The measured spectra are shown in Fig. 6, and SNR greater than 30dB with coding efficiency of 70.47% is measured, by taking the power ratio between in-band signal over the total spectrum power, as power coding efficiency.

In summary, the measurement results show our implemented IFPWM is able to efficiently encode the broadband real communication LTE signals with both high efficiency and good linearity.



(a)



(b)

Fig. 7. (a) Measured power spectrum of 5-level IFPWM power encoded LTE with RF carrier at 1.90464 GHz, and (b) zoomed in-band 20 MHz power spectrum.

IV. Conclusions

A newly developed multi-level intermediate frequency PWM power coding approach targeting for switch-mode PA based fully digital transmitter is introduced. Using a commercial FPGA, we built a 5-level power coding demonstrator which shows measured efficiency above 70%, and SNR>30dB. This is achieved with optimized threshold values for quantization and LUT based pre-distortion function. It is to our best knowledge, the highest measured coding efficiency with LTE signal of 20MHz bandwidth at carrier around 2GHz. The whole procedure is carried out with digital signal processing, eliminating the need for DAC/ADC conversion, thus enables a true software defined radio front end.

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