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TR2014-102 October 2014

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IECON 2014

Space Vector Modulation Method for Modular Multilevel Converters

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***Abstract*—This paper presents a generalized space vector modulation (SVM) method for any modular multilevel converter (MMC). The proposed SVM method produces the maximum level number (i.e., $2n+1$, where n is the number of submodules in the upper or lower arm of each phase) of the output phase voltages and a higher equivalent switching frequency than other modulation methods, which consequently leads to reduced harmonics in the output voltages and currents. Compared with earlier modulation methods for MMCs, the proposed SVM method provides two more degrees of freedom, i.e., the redundant switching sequences and the adjustable duty cycles, thus offering significant flexibility for optimizing the circulating current suppression and capacitor voltage balancing. This SVM method is a useful tool for further studies of MMCs, as it can be conveniently extended for any control objectives. The demonstrated results validate the analysis.**

***Keywords*—space vector modulation (SVM); space vector pulse width modulation (SVPWM); modular multilevel converter (MMC); capacitor voltage balancing; circulating current suppression**

I. INTRODUCTION

There typically exist three conventional topologies for multilevel converters: diode-clamped (neutral-clamped), capacitor-clamped (flying capacitors), and cascaded H-bridge with separate dc sources [1]. Compared with the conventional topologies, the emerging modular multilevel converter (MMC) is considered to be more attractive, due to its significant merits such as modularity and scalability to meet any voltage level requirements [2].

Several pulse width modulation (PWM) methods have been applied to MMCs, and most of them can be classified into two categories, i.e., the carrier-based modulation (including the phase-shifted PWM [3]-[4] and the phase disposition PWM [5]) and the nearest-level modulation [2] [6] methods. Since both of these modulation methods are phase-voltage modulation techniques, they are easy to implement and thus widely adopted. However, the phase-voltage modulation approach results in an inherent drawback of these two modulation methods: sometimes dedicated reference voltages are required in order to achieve a better performance, such as higher modulation indices [6]. In other words, for these modulation methods, the performance of the MMCs is influenced by the selection of the common-mode voltages. The circulating current suppression and capacitor voltage balancing tasks require a more flexible modulation method.

Compared with the abovementioned modulation methods, space vector modulation (SVM) avoids the influence of common-mode voltages by directly controlling the line-to-line voltages, and provides more flexibility to optimize the performance of multilevel converters [2] [7]. Nevertheless, no general SVM method has been introduced to MMCs at this moment. The obstacle for applying SVM to MMCs is the difficulty caused by the largely increased number of switching states and sequences that accompany the higher number of levels. Recently, a fast and generalized SVM method for any conventional multilevel converter has been presented in [7], which generates all the available switching states and switching sequences based on two simple and general mappings, and calculates the duty cycles simply as if for a two-level SVM, thus independent of the level number of the converter. However, the general SVM method in [7] cannot be applied to MMCs directly, due to the different structure and operation principles of MMCs compared to conventional multilevel converters.

This paper extends the modulation method introduced in [7] and proposes a generalized SVM method for any MMC, together with the circulating current and capacitor voltage control. The proposed SVM method has the following salient features:

1) Compared with earlier modulation methods for MMCs, this SVM method provides two more degrees of freedom, i.e., the redundant switching states and the adjustable duty cycles.

2) The highest level number (i.e., $2n+1$, where n is the number of submodules in the upper or lower arm of each phase) of the output phase voltages is achieved, as well as a higher equivalent switching frequency than other modulation methods.

3) It represents a general framework for implementing space vector modulation for MMCs, and can be readily extended for any control objectives.

The rest of the paper is organized as follows: Section II briefly reviews the general SVM scheme introduced in [7]; Section III describes the equivalent model of MMCs and a suggested control method; Section IV presents the proposed SVM method for MMCs; Section V demonstrates some typical results; and Section VI concludes the paper.

II. THE GENERAL SVM SCHEME

Fig. 1 illustrates the general SVM scheme introduced in [7], based on the space vector diagram of a five-level converter. Increasing the level number of the converter by one always forms an additional hexagonal ring of equilateral triangles, which surrounds the outermost hexagon H_0. The principle of this general SVM scheme is briefly explained as follows.

In order to synthesize the reference vector $\boldsymbol{V}_{\text{ref}}$, it is the task of the SVM scheme to detect the modulation triangle $\Delta P_1P_2P_3$ (i.e., the nearest three vectors $\boldsymbol{OP}_1$, $\boldsymbol{OP}_2$, and $\boldsymbol{OP}_3$), to determine the switching sequence (sequence of the nearest three vectors), and to calculate the duty cycles (needed durations) of the nearest three vectors. For a three-phase N-level converter, an output voltage space vector that represents the switching states of all the phases is defined [7] as

$$\boldsymbol{V}_{out} = V_{dc} \cdot (S_a + S_b \cdot e^{j\frac{2}{3}\pi} + S_c \cdot e^{j\frac{4}{3}\pi}) \tag{1}$$

where V_{dc} is the dc-link voltage of the converter; S_{a}, S_{b}, and S_{c} (S_{a}, S_{b}, S_{c}=0, 1, …N-1) are the switching states of phases A, B, and C, respectively. Accordingly, the voltage of phase h (h=A, B, or C) relative to the negative terminal of the dc-link is $S_{\text{h}} \cdot V_{\text{dc}}/(N\text{-}1)$. The definition in (1) makes the side length of each modulation triangle (e.g., $\Delta P_1P_2P_3$) in the space vector diagram to be V_{dc}.

Correspondingly, the reference vector of an N-level converter is generated [7] as

$$\boldsymbol{V}_{ref} = (N-1)\left(V_a^* + V_b^* \cdot e^{j\frac{2}{3}\pi} + V_c^* \cdot e^{j\frac{4}{3}\pi}\right) \tag{2}$$

where V_{a}^*, V_{b}^*, and V_{c}^* are respectively the reference voltages of phases A, B, and C. It is seen that common-mode voltages have no influence on $\boldsymbol{V}_{\text{ref}}$.

Fig. 1(a) shows the detection process of the modulation triangle $\Delta P_1P_2P_3$; a further simplification of the detection will be introduced in future papers. After the equivalent two-level hexagon H_3 that encloses the tip of the reference vector $\boldsymbol{V}_{\text{ref}}$ is detected, the origin of the reference vector is shifted to the center of the two-level hexagon H_3 and a remainder vector $\boldsymbol{V}_{\text{ref}}'$ is generated. Based on the remainder vector $\boldsymbol{V}_{\text{ref}}'$, the switching sequences [e.g., 142 → 141 → 041 → 031 in Fig. 1(b)] and duty cycles are obtained in the same way as for a two-level converter, as shown in Figs. 1(b) and (c). A more detailed explanation for all the symbols in Fig. 1 can be found in [7]. This SVM scheme offers a practical real-time modulation approach for multilevel converters with high level numbers.

Since the first and last switching states (e.g., 142 and 031) in each switching sequence are redundant switching states, their duty cycles can be freely adjusted as long as the summation is a constant [7]. When the reference vector is located in the low modulation regions, a set of redundant switching sequences can be generated [7]. In summary, this general SVM scheme can provide two more degrees of freedom, i.e., the redundant switching sequences and the adjustable duty cycles.

III. EQUIVALENT MODEL AND CONTROL OF MMCS

A. Equivalent Model of MMCs

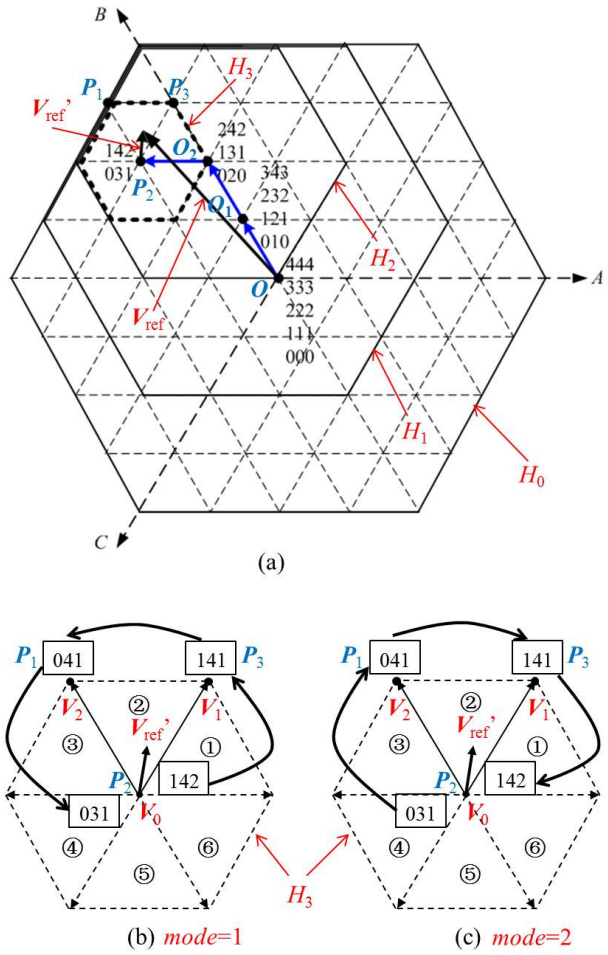

Fig. 1. The SVM method proposed in [7]: (a) detecting the modulation triangle; (b)-(c) two switching sequence modes.

Fig. 2(a) shows the one phase (phase A) structure of an MMC, which contains an upper arm and a lower arm. There are n submodules in each arm (i.e., SM_{aP1}-SM_{aPn} in the upper arm and SM_{aN1}-SM_{aNn} in the lower arm), and a detailed submodule of a half-bridge type is shown in Fig. 2(b). The output voltage v_{SM} of a submodule is v_{C} ("ON" state) when S_1 is switched on and S_2 is switched off, and is zero ("OFF" state) when S_1 is switched off and S_2 is switched on. V_{dc} and i_{dc} are respectively the dc-link voltage and current; i_{ap} and i_{an} are the currents of the upper and lower arm, respectively; and i_{a} is the output current of phase A. The inductors (inductance is L_0) in the upper and lower arms are the buffer inductors; the parasitic ohmic losses in each arm are represented by a resistor R_0.

Based on Kirchhoff's voltage law, the output voltage v_{a} of phase A relative to the negative terminal of the dc-link is respectively calculated for the upper and lower arm as

$$v_a = V_{dc} - u_{ap} - L_0 \cdot di_{ap}/dt - R_0 \cdot i_{ap} \tag{3a}$$

$$v_a = u_{an} + L_0 \cdot di_{an}/dt + R_0 \cdot i_{an} \tag{3b}$$

where u_{ap} and u_{an} are the total output voltage of the submodules in the upper arm and lower arm of phase A, respectively. From (3) and according to Kirchhoff's current law, v_{a} can be obtained as follows

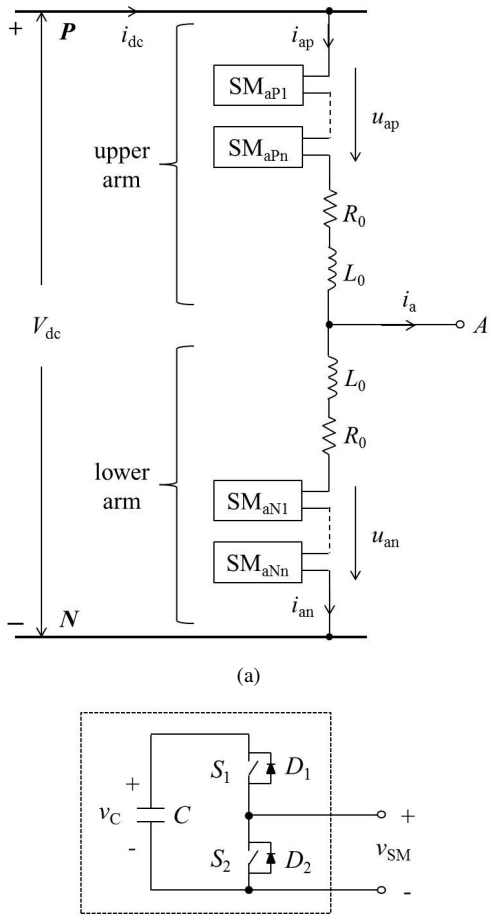

Fig. 2. Basic structure of an MMC: (a) single phase structure; (b) single submodule structure.

$$v_a = v_{a0} - L_0/2 \cdot di_a/dt - R_0/2 \cdot i_a \tag{4a}$$

$$v_{a0} = \left(V_{dc} - u_{ap} + u_{an}\right)/2 \tag{4b}$$

Based on (4), the equivalent circuit of an MMC for the load is depicted in Fig. 3(a), where v_{b0} and v_{c0} are the corresponding voltages of phases B and C similarly defined as in (4b). In this paper, v_{h0} (h=a, b, or c) is called the "modulation voltage".

Fig. 3(a) reveals that an MMC can be modulated according to the reference values of v_{a0}, v_{b0}, and v_{c0}, by substituting them into (1) to generate the reference vector for the general SVM scheme. The general SVM scheme then produces the corresponding switching sequences. The reference value of v_{h0} (h=a, b, or c) is determined in accordance with the load and the applications of the MMC, and can generally be obtained from a current regulator. It is the objective of this paper to determine the appropriate "ON" state submodules for any generated switching sequence, which will be introduced in detail in the next section.

According to Fig. 2, the currents of the upper and lower arm of phase A are [3]

$$i_{ap} = i_{cir,a} + i_a/2 \tag{5a}$$

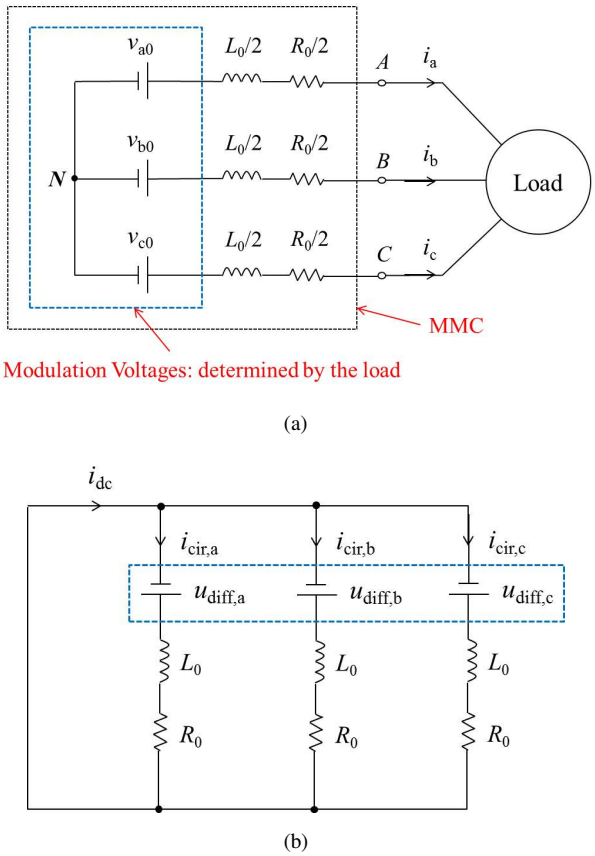

Fig. 3. Equivalent circuit of an MMC: (a) for the load; (b) for the circulating currents.

$$i_{an} = i_{cir,a} - i_a/2 \tag{5b}$$

where $i_{cir,a}$=(i_{ap}+i_{an})/2 is called the circulating current of phase A and is independent of the load. Based on Kirchhoff's voltage law, the circulating current is determined by [8]

$$L_0 \cdot \frac{di_{cir,a}}{dt} + R_0 \cdot i_{cir,a} = u_{diff,a} = \frac{(V_{dc} - u_{ap} - u_{an})}{2} \tag{6}$$

where $u_{diff,a}$ is called the difference voltage of phase A. Accordingly, the equivalent circuit of an MMC for the circulating currents is shown in Fig. 3(b), where $u_{diff,h}$ and $i_{cir,h}$ (h=a, b, or c) are respectively the difference voltage and circulating current of phase h similarly defined in (6). Equation (6) indicates that the circulating current can be suppressed by controlling the corresponding difference voltage.

B. Control of Capacitor Voltages and Circulating Currents

The energy stored in the capacitors of the upper arm (W_{ap}) and the lower arm (W_{an}) of phase A respectively evolve as

$$dW_{ap}/dt = u_{ap} \cdot i_{ap} \tag{7a}$$

$$dW_{an}/dt = u_{an} \cdot i_{an} \tag{7b}$$

By substituting (4)-(6) into the above equations, the derivatives of the total capacitor energy (W_{ap}+W_{an}) of phase A and the unbalanced energy (W_{ap}-W_{an}) between the upper and the lower arms are obtained as

$$\frac{d(W_{ap}+W_{an})}{dt} =$$

$$V_{dc}\cdot(i_{cir,a}+i_a/2) - 2u_{diff,a}\cdot i_{cir,a} - v_{a0}\cdot i_a \quad (8a)$$

$$\frac{d(W_{ap}-W_{an})}{dt} =$$

$$V_{dc}\cdot(i_{cir,a}+i_a/2) - u_{diff,a}\cdot i_a - 2v_{a0}\cdot i_{cir,a} \quad (8b)$$

which show that the circulating current $i_{cir,a}$ plays a significant role for controlling the capacitor energies (i.e., the capacitor voltages in each arm).

As seen in (8a), the dc component of the circulating current corresponds to maintaining the total capacitor energy, by making the dc-link voltage to provide the active power delivered to the load plus the parasitic ohmic losses. On the other hand, (8b) indicates that the unbalanced capacitor energy between the upper and the lower arms can be controlled by regulating the fundamental frequency component of the circulating current that is in phase with the modulation voltage v_{a0}, or the fundamental frequency component of the difference voltage $u_{diff,a}$ that is in phase with the output current i_a. Similar conclusions [8] can be obtained for the other phases.

Fig. 4 shows a control method for capacitor voltages and circulating currents, taking phase A as an example. It consists of three control loops, i.e., the averaging control, the current control, and the arm-balancing control; and finally a reference value $u_{diff,a}^*$ of the difference voltage is generated. Corresponding to (8a), the averaging control forces the average capacitor voltage $\overline{v}_{C,a}$ of the phase to follow its reference value v_C^*, with

$$\overline{v}_{C,a} = (\overline{v}_{C,ap} + \overline{v}_{C,an})/2 \quad (9a)$$

$$\overline{v}_{C,ap} = (\sum_{i=1}^{n} v_{C,api})/n \quad (9b)$$

$$\overline{v}_{C,an} = (\sum_{i=1}^{n} v_{C,ani})/n \quad (9c)$$

where $\overline{v}_{C,ap}$ and $\overline{v}_{C,an}$ are the average capacitor voltages of the upper arm and the lower arm of phase A, respectively; $v_{C,api}$ is the capacitor voltage of the i^{th} submodule in the upper arm; and $v_{C,ani}$ is the capacitor voltage of the i^{th} submodule in the lower arm. The averaging control gives a reference value $i_{cir,a}^*$ of the dc component of the circulating current. According to (6), the current control loop forces the circulating current to follow this reference value, by regulating the dc component of the difference voltage $u_{diff,a}$.

The arm-balancing control loop generates a fundamental frequency component of the difference voltage, to cancel the capacitor voltage difference between the upper and lower arms based on (8b). Note that a low-pass filter (a time constant of 100 ms is used in this paper) is helpful for the arm-balancing control, because the capacitor voltage difference between the two arms contains a considerable fundamental frequency component in steady state [8]. Finally, the reference value $u_{diff,a}^*$ of the difference voltage is generated to achieve the capacitor voltage and circulating current control.

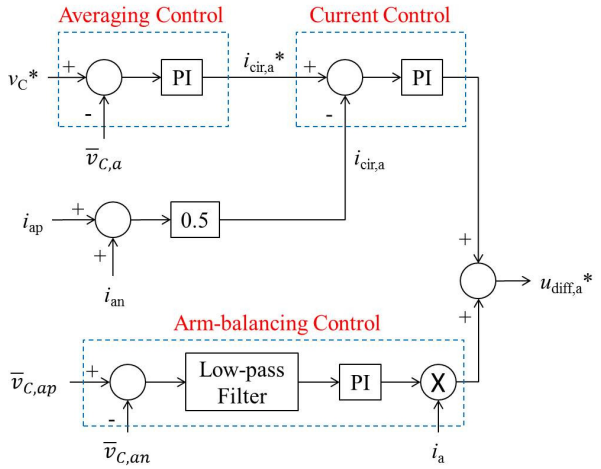

Fig. 4. An example of the capacitor voltage and circulating current control for phase A

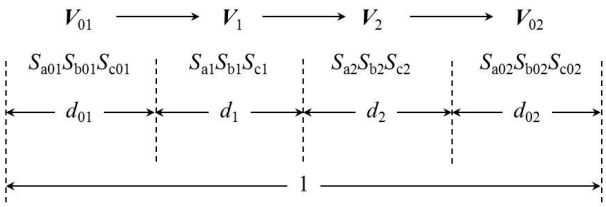

Fig. 5. A switching sequence of the general SVM scheme [7]

IV. Space Vector Modulation for MMCs

A. Generating Reference Voltage for Load

As discussed before for Fig. 3(a), the general SVM scheme introduced in Section II generates the switching sequences, according to any reference values of v_{a0}, v_{b0}, and v_{c0} determined by the load. Fig. 5 shows a switching sequence generated by the general SVM scheme [7]. It consists of four switching states, together with the corresponding duty cycles. Any switching state in the sequence can be represented as $S_aS_bS_c$, where S_h (h=a, b, or c) is the switching state of phase h. The objective of this paper is to select the appropriate submodules at the "ON" state for the upper arm and lower arm of each phase, for each switching state $S_aS_bS_c$ during its duty cycle d.

All the capacitor voltages are assumed to be well balanced in the following analysis, i.e., $v_C = V_{dc}/n$ for any submodule in Fig. 2(b). This proposed SVM method can also be implemented based on another assumption, which will be introduced in a future paper. For the switching state $S_aS_bS_c$, assume k_{hp} and k_{hn} ($0 \le k_{hp}$, $k_{hn} \le n$) submodules respectively in the upper and lower arms of phase h are at the "ON" state. According to (4b), the modulation voltage of phase h is

$$v_{h0} = \left(V_{dc} - k_{hp}\cdot V_{dc}/n + k_{hn}\cdot V_{dc}/n\right)/2 \quad (10)$$

which can also be obtained from (1) as

$$v_{h0} = V_{dc}\cdot S_h/(N-1) \quad (11)$$

where N is the level number of the output phase voltage.

It is shown in (10) that $0 \le v_{h0} \le V_{dc}$ and the minimum voltage step for v_{h0} is $V_{dc}/(2n)$, so theoretically the maximum level number is $N = 2n+1$. From (10) and (11), the following relationship is found

$$n - k_{hp} + k_{hn} = 2n \cdot S_h/(N-1) \tag{12}$$

which ensures that the reference voltage space vector for the load is equivalently generated by the MMC for every switching cycle. Since (12) offers some flexibility of selecting k_{hp} and k_{hn}, this flexibility is used to control the circulating currents and capacitor voltages, as introduced below.

B. Control of Circulating Currents and Capacitor Voltages

As shown in Fig. 4, the controller realizes the circulating current and capacitor voltage control by generating a reference difference voltage for each phase. Note that Fig. 5 is a simplified demonstration of the circulating current and capacitor voltage controller, which if needed can be more sophisticated in order to obtain a better performance. For example, it can be designed to eliminate the even-order circulating harmonic currents through multi-resonant controllers [9] [10]. Other control objectives or approaches can also be applied, such as suppressing the second-order harmonics in the circulating currents based on double line-frequency *acb*-to-*dq* transformation [4]. However, it is always implemented by regulating the $u_{diff,h}^*$ (h=a, b, or c).

Based on the reference difference voltage $u_{diff,h}^*$ obtained for phase h, combining (6) and (12) gives a reference value for k_{hp} and k_{hn} as follows

$$k_{hp}^* = n - \frac{n}{N-1} \cdot S_h - \frac{n}{V_{dc}} \cdot u_{diff,h}^* \tag{13a}$$

$$k_{hn}^* = \frac{n}{N-1} \cdot S_h - \frac{n}{V_{dc}} \cdot u_{diff,h}^* \tag{13b}$$

In order to ensure $0 \le k_{hp} \le n$ and $0 \le k_{hn} \le n$, a general solution for each k_{hi} (i=p or n) is obtained as:

1) If $k_{hi}^* \le 0$,

$$k_{hi} = 0 \tag{14a}$$

2) If $k_{hi}^* \ge n$,

$$k_{hi} = n \tag{14b}$$

3) If $0 < k_{hi}^* < n$,

$$k_{hi} = \begin{cases} \text{int}(k_{hi}^*), & \text{when } 0 < t \le (1-\alpha)d \\ \text{int}(k_{hi}^*) + 1, & \text{when } (1-\alpha)d < t \le d \end{cases} \tag{14c}$$

where $\text{int}(k_{hi}^*)$ represents the integer part of k_{hi}^*, d is the duty cycle of the switching state $S_aS_bS_c$, and

$$\alpha = k_{hi}^* - \text{int}(k_{hi}^*) \tag{15}$$

Fig. 6 illustrates the derivation of (14c): k_{hi}^* is equivalently achieved by two successive integers $\text{int}(k_{hi}^*)$ and $\text{int}(k_{hi}^*)+1$ during the duty cycle d, i.e.,

$$k_{hi}^* \cdot d = \text{int}(k_{hi}^*) \cdot (1-\alpha)d + (\text{int}(k_{hi}^*) + 1) \cdot \alpha d \tag{16}$$

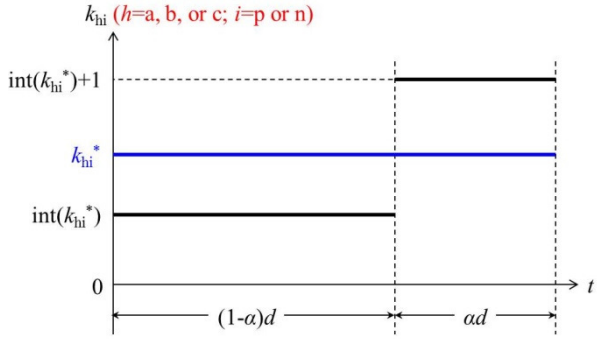

Fig. 6. Generation of k_{hi} (h=a, b, or c; i=p or n) for the switching state S_h within its duty cycle d

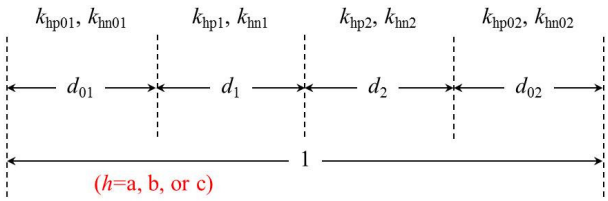

Fig. 7. A set of k_{hp} and k_{hn} (h=a, b, or c) for the switching sequence shown in Fig. 5

Consequently, a set of k_{hp} and k_{hn} are determined according to each switching state for every switching sequence, as shown in Fig. 7. The k_{hp} and k_{hn} obtained from (14) force the difference voltage of phase h (h=a, b, or c) to be $u_{diff,h}^*$, and therefore achieve the control of circulating currents and capacitor voltages. Since $u_{diff,h}^*$ is updated for every switching state in accordance with the circulating currents and the capacitor voltages, this SVM method offers a better control performance than other modulation methods because of the higher equivalent switching frequency.

C. Selection of Submodules

After k_{hp} and k_{hn} of phase h (h=a, b, or c) are obtained for each switching state, the capacitor voltages of the submodules in each arm are balanced by selecting the appropriate ON-state submodules according to the direction of the arm current, called the sorting method [6]. The basic principle is:

1) If the arm current is positive, the submodules with the lowest capacitor voltages are selected to be ON-state, because the capacitors of these submodules are charged.

2) If the arm current is negative, the submodules with the highest capacitor voltages are selected to be ON-state, because the capacitors of these submodules are discharged.

In order to reduce the switching transitions or the time consumption caused by the sorting, several improvements have been introduced to the sorting method [4] [11], which can also be applied to this proposed SVM method. The sorting method ensures the capacitor voltages in each arm to be identical. Together with the voltage/energy control loops shown in Fig. 4, it makes the capacitor voltages of different arms to be also balanced, without requiring large capacitors.

The ON-state submodules are consequently determined for each switching sequence, corresponding to the set of k_{hp} and k_{hn} shown in Fig. 7. Note that the general SVM scheme introduced in Section II can provide two more degrees of freedom, i.e., the

redundant switching states and the adjustable duty cycles [7]. Both of these degrees of freedom can be employed to optimize the capacitor voltage balancing and circulating current suppression, because different switching states (which lead to different k_{hp} and k_{hn}) or duty cycles cause different influence on the capacitor voltages and the circulating currents.

D. Summary

Fig. 8 illustrates the diagram of this proposed SVM method, which represents a general framework for implementing space vector modulation for MMCs. It can be conveniently extended for any control objectives, by replacing the circulating current and capacitor voltage control block with customized controllers.

V. Results

Simulations are carried out in this section to demonstrate the proposed SVM method, based on an MMC with the parameters summarized in Table I.

Fig. 9 depicts the transient performance of this SVM method when the voltage level number is N=9 (i.e., the maximum value $2n$+1): the modulation index is dropped from 0.9 to 0.6 at t=0.2 s. Shown in Fig. 9(a) are the capacitor voltages $v_{C,ap1}$ and $v_{C,an1}$ respectively in the upper and lower arms, which indicate the overall balancing of the capacitor voltages. Fig. 9(b) presents the phase and arm currents i_a, i_{ap} and i_{an}.

To observe the influence of voltage level numbers, Figs. 10(a) and (b) give the modulation voltage v_{a0} of phase A when N=9 and N=5, respectively. The corresponding harmonic spectrum and total harmonic distortion (THD) are shown in Figs. 10(c) and (d), which reveal that the higher voltage level number leads to reduced harmonics in the output voltage. Since this SVM method can produce the maximum number of voltage levels, it results in fewer harmonic contents of the output voltages and currents, compared with other modulation methods.

VI. Conclusion

This paper proposes a general space vector modulation (SVM) method for any modular multilevel converter (MMC), which has the following salient features:

1) Compared with earlier modulation methods for MMCs, this

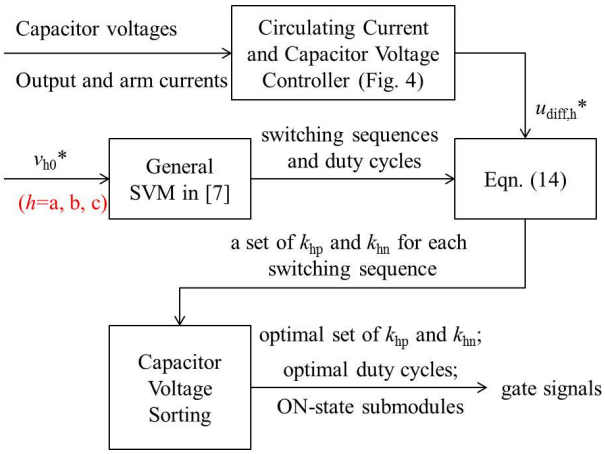

Fig. 8. The SVM method for MMCs proposed in this paper

TABLE I. Parameters of the MMC (Base Case)

DC-link voltage (V_{dc})	800 V
No. of submodules per arm (n)	4
Submodule capacitor voltage (v_C)	200 V
Submodule capacitance (C)	2.2 mF
Buffer inductance (L_0)	10 mH
Parasitic resistor in each arm (R_0)	88.88 mΩ
Load inductance (L_L)	10 mH
Load resistance (R_L)	20 Ω
Switching frequency (f_s)	5 kHz
Fundamental frequency (f_0)	50 Hz
Modulation index (m)	0.9
Voltage level number (N)	9

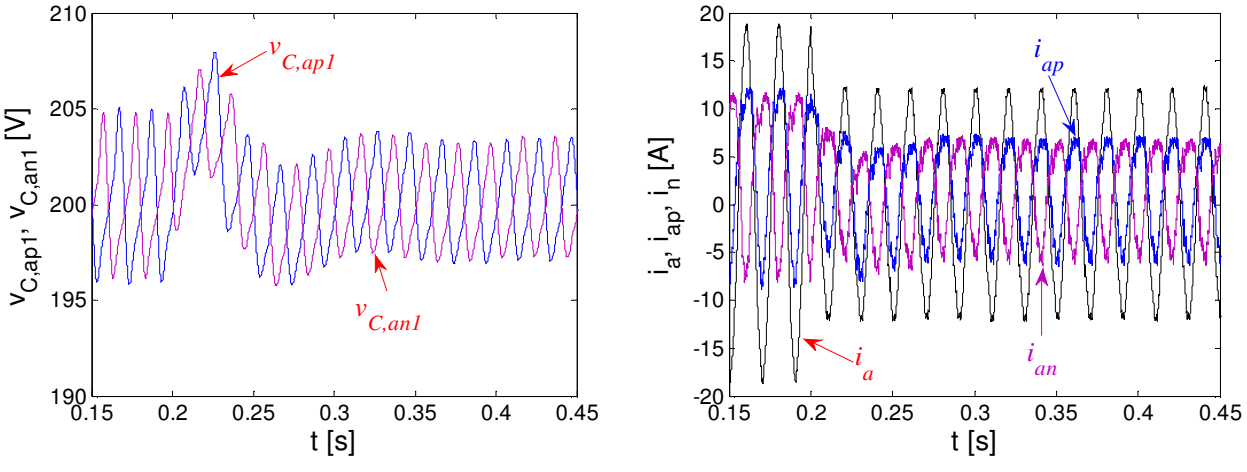

Fig. 9. Transient performance (m is dropped from 0.9 to 0.6 at t=0.2 s) of this SVM method: (a) capacitor voltages $v_{C,ap1}$ and $v_{C,an1}$; (b) currents i_a, i_{ap} and i_{an}.

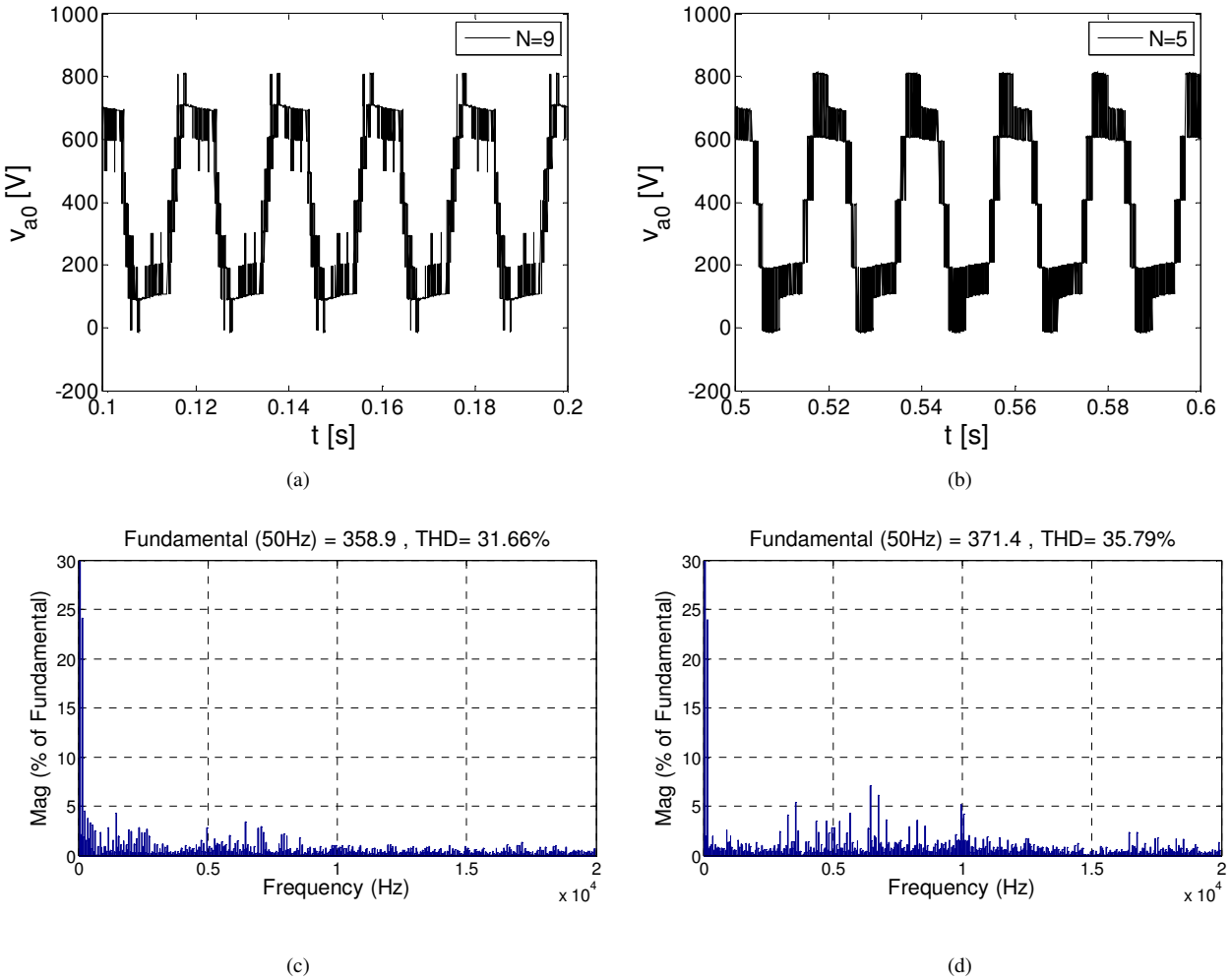

Fig. 10. Simulation results for different voltage level numbers [N=9 for (a) and (c); N=5 for (b) and (d)]: (a)-(b) modulation voltage v_{a0} of phase A; (c)-(d) harmonic spectrum and total harmonic distortion (THD) of v_{a0}.

SVM method provides two more degrees of freedom, i.e., the redundant switching states and the adjustable duty cycles.

2) The highest level number (i.e., $2n$+1, where n is the number of submodules in the upper or lower arm of each phase) of the output phase voltages is achieved, as well as a higher equivalent switching frequency than other modulation methods.

3) It represents a general framework for implementing space vector modulation for MMCs, and can be conveniently extended for any control objectives.

These advantages of this SVM method make it a useful tool for further studies of MMCs.

REFERENCES

[1] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[2] Y. Deng and R. G. Harley, "Space-Vector versus Nearest-Level Pulse Width Modulation for Multilevel Converters," *IEEE Trans. Power Electron.*, vol. PP, no. 99, pp. 1, 2014.

[3] M. Hagiwara and H. Akagi, "Control and experiment of pulse width modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

[4] Q. Tu, Z. Xu, and L. Xu, "Reduced Switching-Frequency Modulation and Circulating Current Suppression for Modular Multilevel Converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

[5] J. Mei, B. Xiao, et al., "Modular Multilevel Inverter with New Modulation Method and Its Application to Photovoltaic Grid-Connected Generator," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5063-5073, Nov. 2013.

[6] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2633-2642, Aug. 2010.

[7] Y. Deng, K. H. Teo, C. Duan, T. G. Habetler, and R. G. Harley, "A Fast and Generalized Space Vector Modulation Scheme for Multilevel Inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5204-5217, Oct. 2014.

[8] A. Antonopoulos, L. Angquist, and H. P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *Proc. Eur. Conf. Power Electron.*, Sept. 2009, pp. 1-10.

[9] Z. Li, P. Wang, et al., "An Inner Current Suppressing Method for Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4873-4879, Nov. 2013.

[10] M. Zhang, L. Huang, W. Yao, and Z. Lu, "Circulating Harmonic Current Elimination of a CPS-PWM-Based Modular Multilevel Converter With a Plug-In Repetitive Controller," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2083–2097, Apr. 2014.

[11] J. Qin and M. Saeedifard, "Reduced Switching-Frequency Voltage-Balancing Strategies for Modular Multilevel HVDC Converters," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2403-2410, Oct. 2013.