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TR2015-048 March 2016

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IEEE Transactions on Power Electronics

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication.

A Simplified Space Vector Modulation Scheme for Multilevel Converters

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***Abstract*—This paper proposes a simplified space vector modulation (SVM) scheme for multilevel converters. Compared with earlier SVM methods, the proposed scheme simplifies the detection of the nearest three vectors and the generation of switching sequences, and therefore is computationally more efficient. Particularly, for the first time, the proposed scheme achieves the same easy implementation as phase-voltage modulation techniques. Another superior characteristic of the proposed scheme over earlier methods is its potential for multiphase multilevel applications. The proposed scheme also offers the following significant advantages: 1) independence of the level number of the converter; 2) more degrees of freedom, i.e., redundant switching sequences and adjustable duty cycles, to optimize the switching patterns; and 3) no need for lookup tables or coordinate transformations. These advantages make the proposed scheme well suited to large level-number applications, such as modular multilevel converters (MMCs) and high voltage direct current (HVDC) systems. Simulation and experimental results verify this new concept.**

***Index Terms*—Space vector modulation (SVM); space vector pulse width modulation (SVPWM); multilevel converter; multilevel inverter; modular multilevel converter (MMC); high voltage direct current (HVDC); multiphase converter; orthogonal unit-vectors.**

I. Introduction

Multilevel converters demonstrate various advantages compared to two-level converters, such as reduced voltage stress on the power devices, lower harmonics, and lower instantaneous rate of voltage change (*dv*/*dt*) [1]. During the past decades, three basic topologies have been proposed for multilevel converters: diode-clamped (neutral-clamped) [2]-[4], capacitor-clamped (flying capacitors) [5], and cascaded H-bridge with separate dc sources [6]. Another emerging topology called the modular multilevel converter (MMC) was introduced in the early 2000s [7], which has recently been shown to be even more promising for high-voltage/power applications, due to its significant merits such as modularity and scalability to meet any voltage level requirements [8]-[10]. For example, the first commercialized MMC-based high voltage direct current (HVDC) system, i.e., the "Trans Bay Cable Project", is reported to have achieved ±200 kV/400 MW and 216 voltage-levels [11].

Many pulse width modulation (PWM) methods have been developed for multilevel converters, and most of them can be classified into three typical categories: 1) carrier-based modulation [12], including phase-shifted PWM [13]-[16] and phase-disposition PWM [17]-[19]; 2) nearest-level modulation [20]-[24], which is extended from a nearest-level-control method [25] [26] by introducing the PWM operation; and 3) space vector modulation (SVM) [27]-[32]. SVM works with line-to-line voltages (i.e., it simultaneously deals with all phases), while the other two methods are phase-voltage modulation techniques. Since SVM eliminates the influence of common-mode voltages and avoids the use of any triangular carrier wave, it conveniently provides more flexibility (i.e., redundant switching sequences and adjustable duty cycles) to optimize switching waveforms [24] [32], and is more suited to digital implementations. These advantages of SVM can lead to a significantly improved performance of multilevel converters, especially when the level number of the converter is large (e.g., 216 voltage-levels in the "Trans Bay Cable Project"), because a larger level number facilitates a higher redundancy and therefore more potential for optimization.

However, in spite of its distinct advantages, SVM for four or higher level converters is difficult. There generally are n^3 switching states and $6(n\text{-}1)^2$ triangles in the space vector diagram of a three-phase n-level converter [32]; a reference vector can be located within any triangle. To achieve the same volt-second average as the reference vector, it is the task of SVM to select suitable switching states of the located triangle (its vertices are the "nearest three vectors") and execute them for respective needed durations (duty cycles) in an appropriate sequence (switching sequence). Fig. 1 shows the functional diagram of an SVM-based three-phase n-level converter, where the single-pole n-throw switch represents the functionality of each converter phase. In order to carry out the real-time control for a converter with a large number of levels (e.g., in HVDC applications), an SVM scheme is required to be easily implementable and computationally efficient. Nevertheless, none of the earlier SVM methods [27]-[32] is well suited to those requirements.

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The SVM algorithm presented in [27] is based on a 60º coordinate system. When a reference vector is provided in the stationary reference frame (α-β coordinates), this unusual 60º coordinate system requires several matrix transformations, and therefore causes extra computational burden. More critically, [27] does not provide a systematic approach for determining the switching sequences. Some studies [33] [34] attempt to solve this problem by using the phase-disposition PWM. Because of the inherent drawbacks of the carrier-based method (e.g., carrier waves and selected common-mode voltages are needed), this approach not only increases the complexity, but also undermines the flexibility [24]. Sometimes even the carrier waves are required to be sophisticatedly modified for each switch [34], in order to achieve the optimized switch utilization. This is challenging in real applications, especially when the converter consists of a large number of switches.

The methods in [28] and [29] are basically two different representations of the algorithm in [27]. Both methods avoid the unconventional 60º coordinate system, based on a transformation of the reference vector [35] and a transformed α-β coordinate frame [29], respectively. However, neither of the two methods provides a systematic approach to determining the switching sequences, similar to [27]. Moreover, compared to the algorithm in [27], the following extra complexity emerges in the two methods: 1) the sector location of the reference vector needs to be detected in [28], because different sectors apply different formulas for the switching states and duty cycles; 2) the method in [29] requires more operations when recovering the three-dimensional switching sates from the coordinates in the transformed α-β frame.

In [30], a two-level SVM based scheme is described. It consists of a primary unit and a secondary unit. The primary unit identifies the triangle that encloses the tip of the reference vector, determines a small vector for a virtual two-level converter, and then obtains the duty cycles based on a two-level SVM. An advantage of this method is that the calculation of duty cycles is independent of the level number. On the contrary, the secondary unit requires a pre-stored switching sequence mapping table to determine the switching states and sequences, which is significantly influenced by the level number of the converter. Since the number of available switching sequences increases rapidly with the higher number of levels, more memory will be needed and a slower mapping speed will be achieved when this method is applied to higher level converters. In fact, the memory required to store the switching states for an n-level converter is $3n^3(n\text{-}1)/8$ bytes [30].

Another method based on the concept of two-level SVM is introduced in [31]. To detect the center of a two-level hexagon that contains the tip of the reference vector, a so called "distance term" needs to be calculated and compared for each vector on the inner side of a particular layer (i.e., the hexagonal ring where the reference vector is located). This iterative operation will lead to considerable computation time when the level number of the converter is large, because more vectors exist in the space vector diagram. An extra two-phase to three-phase conversion is also required to identify the particular layer, since most control schemes give a reference vector in two-dimensional coordinates. Moreover, in this method some switching states and sequences that are actually suitable for the reference vector are ignored, which causes the method to not provide optimal switching waveforms for every operation condition.

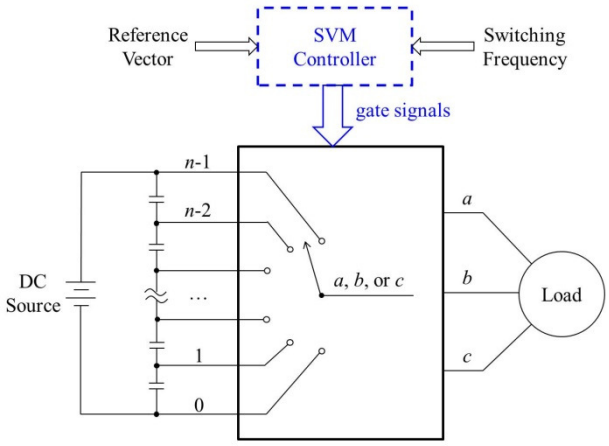

Fig. 1. Functional diagram of a three-phase n-level converter

TABLE I

COMPARISON OF EARLIER SVM AND THE OTHER TWO MODULATION METHODS

	Comparison
Flexibility	SVM > nearest-level modulation > carrier-based modulation
Ease of implementation	nearest-level modulation > carrier-based modulation > SVM

The general n-level scheme in [32], for the first time, proposes a systematic approach to easily determine all the available switching sequences. The basic idea is virtually reducing the level number of the converter, until a two-level hexagon that encircles the vertex of the reference vector is identified; the shifting of vectors is represented by adjusting the switching states of the corresponding phase. Finally, this scheme calculates the duty cycles simply as if for a two-level SVM, and generates all the available switching states and sequences based on two simple and general mappings. No lookup table or coordinate transformation is needed. However, the detection of the two-level hexagon is achieved by determining a set of nested hexagons, which is dependent on the level number and requires iterative calculations. These iterative calculations reduce the computational efficiency of the scheme when the level number is large. Moreover, because of the encoding (which causes complexity and extra memory consumption in real-time implementation) needed for the four switching states and the respective duty cycles in each switching sequence, the proposed approach of generating switching sequences is still relatively more complicated than

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the other two types of modulation methods.

In summary, there exist non-ignorable drawbacks in each of the earlier SVM methods [27]-[32]. Table I summarizes the comparison between earlier SVM and the other two modulation methods, in terms of flexibility and ease of implementation [24]. Because of its complicated implementation, SVM is less frequently adopted for large level numbers (such as MMC and HVDC applications [11] [36]), in spite of its significant flexibility. Furthermore, none of the earlier SVM methods [27]-[32] are capable of dealing with increasingly employed multiphase multilevel converters [37] [38]. For example, the 60º coordinate system in [27] is specific to three-phase systems, and cannot be extended to other multiphase applications. A further simplified and generalized SVM scheme is therefore needed.

This paper proposes a new SVM scheme for multilevel converters. Both the detection of the nearest three vectors and the generation of switching sequences are extremely simplified. The proposed scheme has the following salient advantages:

1) It is independent of the level number of the converter, and is computationally more efficient than earlier SVM methods.
2) This scheme achieves the same easy implementation as the nearest-level modulation, while maintaining significant flexibility (i.e., redundant switching sequences and adjustable duty cycles). Therefore, it is well suited to large level-number applications (e.g., MMC and HVDC).
3) No lookup table or coordinate transformation is required. The scheme is based on the α-β coordinates.
4) The proposed scheme can potentially be extended to multiphase applications.

The rest of this paper is organized as follows: Section II introduces a general approach to construct orthogonal unit-vectors to decouple different phases; Section III presents the proposed simplified SVM scheme for any multilevel converter; Section IV demonstrates some typical simulation and experimental results; and Section V concludes the paper.

II. Orthogonal Unit-Vectors

This section introduces a general approach to construct orthogonal unit-vectors for different multiphase systems, as illustrated in Fig. 2. The objective is to decouple the components of different phases, so as to implement the SVM based on the commonly-used α-β coordinates.

A. Three-Phase System

For the three-phase n-level converter shown in Fig. 1, a reference vector is generated [24] [32] as

$$\boldsymbol{V}_{ref} = (n-1)\left(V_a^* + V_b^* \cdot e^{j\frac{2}{3}\pi} + V_c^* \cdot e^{j\frac{4}{3}\pi}\right)$$

$$= (n-1)\left(m \cdot \frac{\sqrt{3}}{2} V_{dc} \cdot e^{j\theta}\right) \quad (1)$$

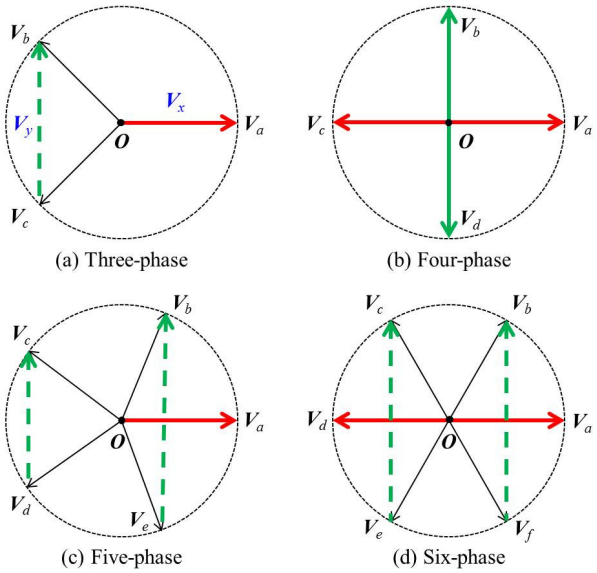

Fig. 2. Orthogonal unit-vectors for different multiphase systems

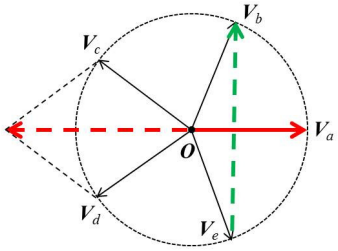

Fig. 3. Another two orthogonal unit-vectors for the five-phase system

where V_a^*, V_b^*, and V_c^* are respectively the reference voltages of phases a, b, and c relative to the negative terminal of the dc-link; V_{dc} is the dc-link voltage of the converter; m is the modulation index; and θ is the phase angle of the phase a voltage. According to (1), any reference vector is constructed by three "unit-vectors" $\boldsymbol{V}_a$, $\boldsymbol{V}_b$, and $\boldsymbol{V}_c$ of the three phases, where

$$\begin{bmatrix} \boldsymbol{V}_a \\ \boldsymbol{V}_b \\ \boldsymbol{V}_c \end{bmatrix} = V_{dc} \cdot \begin{bmatrix} 1 \\ e^{j\frac{2}{3}\pi} \\ e^{j\frac{4}{3}\pi} \end{bmatrix} \quad (2)$$

The coupling of the three-phase components, when composing the reference vector, leads to the difficulty in detecting the positions of the nearest three vectors. If the reference vector can be decomposed into orthogonal coordinates, where the component of each phase is only contained in one of the coordinates (i.e., the three phases are "decoupled"), then the component related to each phase can be directly obtained from the decomposition. As shown in Fig. 2(a), two such orthogonal unit-vectors $\boldsymbol{V}_x$ and $\boldsymbol{V}_y$ corresponding to the real and imaginary axes (i.e., the α-β frame) are defined as

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$$\begin{bmatrix} \boldsymbol{V}_x \\ \boldsymbol{V}_y \end{bmatrix} = \begin{bmatrix} \boldsymbol{V}_a \\ \boldsymbol{V}_b - \boldsymbol{V}_c \end{bmatrix} = V_{dc} \cdot \begin{bmatrix} 1 \\ j\sqrt{3} \end{bmatrix} \tag{3}$$

The basic concept of constructing these orthogonal unit-vectors can be summarized as follows: 1) a unit-vector in the direction of the real or imaginary axis is already an orthogonal component; 2) if a unit-vector is not laid on the real or imaginary axis, then it can be combined with another unit-vector (these two unit-vectors are symmetrical with respect to the real or imaginary axis) to compose an orthogonal component.

According to the two orthogonal unit-vectors $\boldsymbol{V}_x$ and $\boldsymbol{V}_y$, the real and imaginary coordinates (i.e., x and y, respectively) of the reference vector $\boldsymbol{V}_{ref}$ are

$$x = \frac{V_{ref(x)}}{V_{dc}}, \quad y = \frac{V_{ref(y)}}{\sqrt{3}V_{dc}} \tag{4}$$

where $V_{ref(x)}$ and $V_{ref(y)}$ are respectively the real and imaginary components of the reference vector. When $\boldsymbol{V}_{ref}$ is located in over-modulation regions, it can be modified similarly as in [32].

Afterwards, based on the definition of $\boldsymbol{V}_x$ and $\boldsymbol{V}_y$ in (3), a new set of reference voltages for the three phases can be easily obtained as follows (though not actually needed in the proposed scheme) from the reference vector as a reverse process:

$$\begin{bmatrix} V_{a0}^* \\ V_{b0}^* \\ V_{c0}^* \end{bmatrix} = \frac{1}{n-1} \begin{bmatrix} x \cdot V_{dc} \\ y \cdot V_{dc} \\ -y \cdot V_{dc} \end{bmatrix} = \frac{1}{n-1} \begin{bmatrix} V_{ref(x)} \\ V_{ref(y)}/\sqrt{3} \\ -V_{ref(y)}/\sqrt{3} \end{bmatrix} \tag{5}$$

For an SVM scheme, this new set of reference voltages $\{V_{a0}^*, V_{b0}^*, V_{c0}^*\}$ is equivalent to the original reference voltage set $\{V_a^*, V_b^*, V_c^*\}$ in (1), as they generate the same reference vector.

B. Multiphase System

The aforementioned concept of constructing the orthogonal unit-vectors can be easily extended to other multiphase systems. For example, Fig. 2 also demonstrates the orthogonal unit-vectors for four-, five-, and six-phase systems, where the bolded arrows represent the orthogonal components (the dashed arrows are composed by two unit-vectors).

The orthogonal unit-vectors for four-, five-, and six-phase systems are respectively as follows

$$\begin{bmatrix} \boldsymbol{V}_{x4} \\ \boldsymbol{V}_{y4} \end{bmatrix} = \begin{bmatrix} \boldsymbol{V}_a - \boldsymbol{V}_c \\ \boldsymbol{V}_b - \boldsymbol{V}_d \end{bmatrix} = V_{dc} \cdot \begin{bmatrix} 2 \\ j2 \end{bmatrix} \tag{6a}$$

$$\begin{bmatrix} \boldsymbol{V}_{x5} \\ \boldsymbol{V}_{y5} \end{bmatrix} = \begin{bmatrix} \boldsymbol{V}_a \\ \boldsymbol{V}_b - \boldsymbol{V}_e + \boldsymbol{V}_c - \boldsymbol{V}_d \end{bmatrix} = V_{dc} \cdot \begin{bmatrix} 1 \\ j2(\sin(0.2\pi) + \sin(0.4\pi)) \end{bmatrix} \tag{6b}$$

$$\begin{bmatrix} \boldsymbol{V}_{x6} \\ \boldsymbol{V}_{y6} \end{bmatrix} = \begin{bmatrix} \boldsymbol{V}_a - \boldsymbol{V}_d \\ \boldsymbol{V}_b - \boldsymbol{V}_f + \boldsymbol{V}_c - \boldsymbol{V}_e \end{bmatrix} = V_{dc} \cdot \begin{bmatrix} 2 \\ j2\sqrt{3} \end{bmatrix} \tag{6c}$$

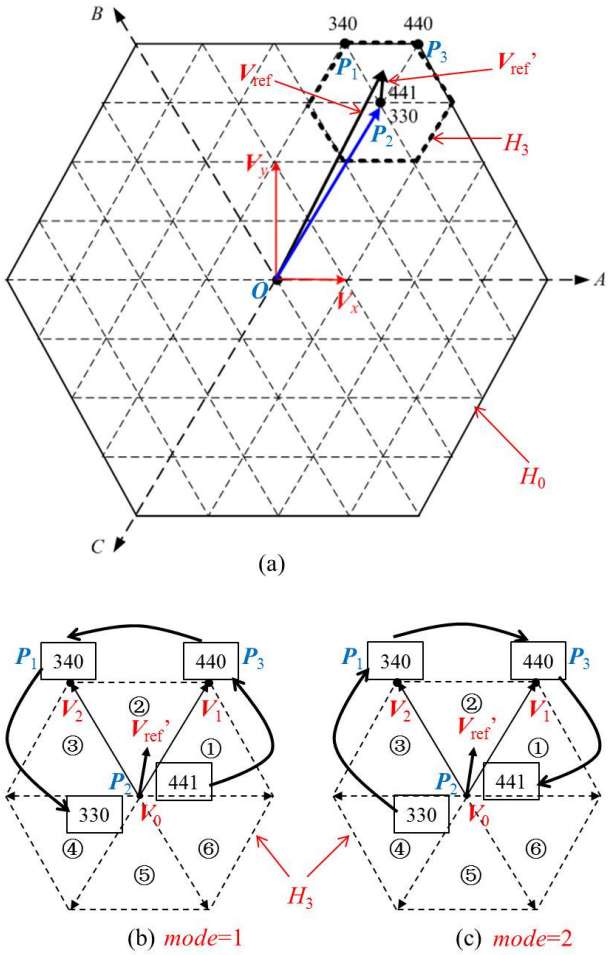

Fig. 4. The proposed SVM scheme: (a) detecting the modulation triangle; (b)-(c) two switching sequence modes.

Note that the orthogonal unit-vectors may be constructed in different ways. For example, Fig. 3 shows another candidate choice of the orthogonal unit-vectors for the five-phase system:

$$\begin{bmatrix} \boldsymbol{V}'_{x5} \\ \boldsymbol{V}'_{y5} \end{bmatrix} = \begin{bmatrix} \boldsymbol{V}_a - \boldsymbol{V}_c - \boldsymbol{V}_d \\ \boldsymbol{V}_b - \boldsymbol{V}_e \end{bmatrix} = V_{dc} \cdot \begin{bmatrix} 1 + 2\cos(0.2\pi) \\ j2\sin(0.4\pi) \end{bmatrix} \tag{7}$$

Similar to the discussion in (5), the equivalent reference voltages for all the phases can always be recovered as a reverse process, no matter what set of orthogonal unit-vectors is adopted. Therefore, the different constructions of orthogonal unit-vectors have no influence on the accuracy.

III. Proposed SVM Scheme

Fig. 4 shows the proposed n-level SVM scheme, based on the space vector diagram of a five-level converter. Increasing the level number by one always forms an additional hexagonal ring of equilateral triangles, which surrounds the outermost hexagon H_0. Fig. 4 is explained later in detail. The proposed scheme works for all the multilevel converter topologies (i.e., diode/capacitor-clamped, cascaded H-bridge, and MMC), since they have the same space vector diagram.

Corresponding to (1), an output space vector that represents the switching states of all the phases is defined for a three-phase n-level converter [24] [32] as

$$\boldsymbol{V}_{out} = V_{dc} \cdot \left(S_a + S_b \cdot e^{j\frac{2}{3}\pi} + S_c \cdot e^{j\frac{4}{3}\pi} \right) \tag{8}$$

where S_a, S_b, and S_c (S_a, S_b, S_c=0, 1, …n-1) are the switching states of phases a, b, and c, respectively. Accordingly, the voltage of phase h (h=a, b, or c) relative to the negative terminal of the dc-link is $S_h \cdot V_{dc}/(n\text{-}1)$. The definition in (8) causes the side length of each modulation triangle (e.g., $\Delta P_1P_2P_3$) in the space vector diagram to be V_{dc}.

All the output space vectors of the converter compose the space vector diagram, where the number at each vertex (e.g., 340 at P_1) represents the switching state $S_aS_bS_c$ of the corresponding space vector. Some space vectors can be equivalently produced by more than one switching state; those switching states are called redundant switching states, and are listed decreasingly from top to bottom corresponding to the switching states of phase a. For example, 441 and 330 are both valid switching states of the space vector $\boldsymbol{OP}_2$.

In order to synthesize the reference vector $\boldsymbol{V}_{ref}$ defined in (1), it is the task of the SVM scheme to detect the modulation triangle $\Delta P_1P_2P_3$ (i.e., the nearest three vectors $\boldsymbol{OP}_1$, $\boldsymbol{OP}_2$, and $\boldsymbol{OP}_3$), to calculate the duty cycles (needed durations) of the nearest three vectors, and to determine the switching sequence (switching state sequence of the nearest three vectors). The synthesis is based on achieving the same volt-second average [24] [32]

$$\boldsymbol{V}_{ref} = D_1 \cdot \boldsymbol{OP}_1 + D_2 \cdot \boldsymbol{OP}_2 + D_3 \cdot \boldsymbol{OP}_3 \tag{9}$$

where D_1, D_2, and D_3 are the duty cycles of $\boldsymbol{OP}_1$, $\boldsymbol{OP}_2$, and $\boldsymbol{OP}_3$, respectively. Normally, to ensure the minimum number of switch transitions in every switching cycle, the optimized switching sequences [24] [32] [33] are required.

A. *Detecting the Nearest Three Vectors*

It should be noted that unlike earlier SVM methods, only one of the nearest three vectors (e.g., $\boldsymbol{OP}_2$) needs to be detected in the proposed scheme. A simple mapping subsequently generates the switching sequences, based on the detected nearest vector. An alternative way to directly detect all the nearest three vectors is introduced in the Appendix.

The two orthogonal unit-vectors $\boldsymbol{V}_x$ and $\boldsymbol{V}_y$ defined in (3) are illustrated in Fig. 4(a). According to these two orthogonal unit-vectors, the real and imaginary coordinates of the reference vector $\boldsymbol{V}_{ref}$ (i.e., x and y, respectively) are obtained from (4). Afterwards, the vertex (i.e., P_2 as in Fig. 4) of the modulation triangle $\Delta P_1P_2P_3$, that is closest to the origin O of the space vector diagram, can be easily detected as follows.

At first, it is observed from (3) that the three-dimensional coordinates (i.e., corresponding to the three unit-vectors $\boldsymbol{V}_a$, $\boldsymbol{V}_b$, and $\boldsymbol{V}_c$ in the original ABC-frame) of the two orthogonal unit-vectors $\boldsymbol{V}_x$ and $\boldsymbol{V}_y$ are $[1, 0, 0]^T$ and $[0, 1, -1]^T$, respectively. Therefore, a three-dimensional coordinate of the reference vector $\boldsymbol{V}_{ref}$ is $[x, y, -y]^T$, as discussed in (5). Since $\boldsymbol{V}_a + \boldsymbol{V}_b + \boldsymbol{V}_c = \boldsymbol{0}$, equally adjusting the three components of $[x, y, -y]^T$ generates another three-dimensional coordinate of $\boldsymbol{V}_{ref}$. The objective is to select an appropriate adjustment, so as to easily detect the switching states of a nearest vector.

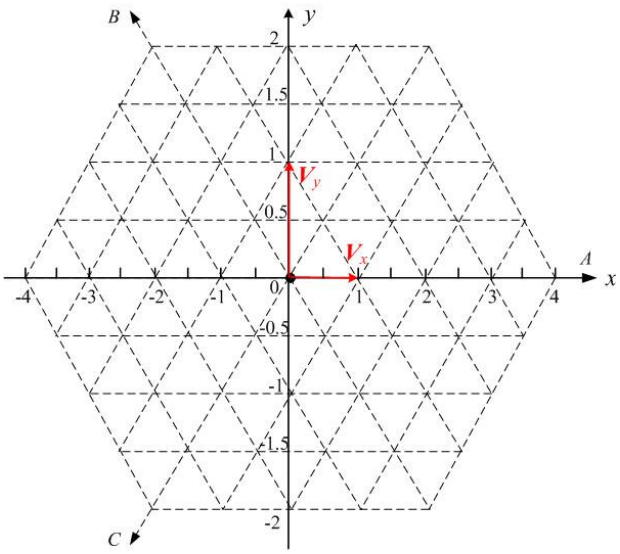

Fig. 5. Coordinates of the space vectors according to the orthogonal unit-vectors $\boldsymbol{V}_x$ and $\boldsymbol{V}_y$

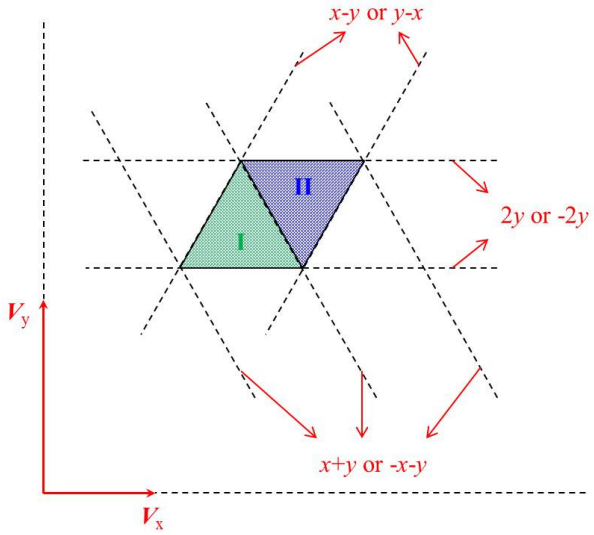

Fig. 6. Limits of x-min(x, y, -y), y-min(x, y, -y), and -y-min(x, y, -y)

Consequently, a candidate switching state $S_aS_bS_c$ for the vertex (i.e., P_2) of the modulation triangle $\Delta P_1P_2P_3$ closest to the origin is directly obtained as

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \text{int}\left(\begin{bmatrix} x - \min(x, y, -y) \\ y - \min(x, y, -y) \\ -y - \min(x, y, -y) \end{bmatrix} \right) \tag{10}$$

where min(x, y, -y) denotes the minimum value among x, y, and -y; int(γ) stands for the corresponding integer parts of all the elements in an array γ. Note that the computational burden of (10) is independent of the level number of the converter or the location of the reference vector.

The rationale for (10) can be explained as follows. Wherever the reference vector is located, the candidate switching state $S_aS_bS_c$ only has the following values:

$$\begin{bmatrix}S_a\\S_b\\S_c\end{bmatrix} = \text{int}\left(\begin{bmatrix}0\\y-x\\-y-x\end{bmatrix}\right), \quad \text{if } \min(x,y,-y)=x \tag{11a}$$

$$\begin{bmatrix}S_a\\S_b\\S_c\end{bmatrix} = \text{int}\left(\begin{bmatrix}x-y\\0\\-2y\end{bmatrix}\right), \quad \text{if } \min(x,y,-y)=y \tag{11b}$$

$$\begin{bmatrix}S_a\\S_b\\S_c\end{bmatrix} = \text{int}\left(\begin{bmatrix}x+y\\2y\\0\end{bmatrix}\right), \quad \text{if } \min(x,y,-y)=-y \tag{11c}$$

Fig. 5 shows the coordinates of the space vectors according to $\boldsymbol{V}_x$ and $\boldsymbol{V}_y$. An important fact is seen from Fig. 5 that x-min(x, y, -y), y-min(x, y, -y), and -y-min(x, y, -y) are all integers for the three vertices of any modulation triangle. In the coordinate system with the basis set {$\boldsymbol{V}_x$, $\boldsymbol{V}_y$}, there are two types of modulation triangles (i.e., the upward "I" and the downward "II" triangles as in Fig. 6) in the space vector diagram. Fig. 6 shows that for an area enclosed by either type of modulation triangle, x-min(x, y, -y), y-min(x, y, -y), and -y-min(x, y, -y) produce their maximum and minimum values at the three vertices of the triangle; the difference between the maximum and the corresponding minimum value is always one. Therefore, the candidate switching state obtained from (10) gives the result of one nearest vector, regardless of the location of the reference vector.

Due to the adoption of min(x, y, -y), this detected vector is the vertex of the modulation triangle that is closest to the origin. Fig. 7 illustrates the nearest vector detected by (10) for different locations of the reference vector according to (11), where Q_1 and Q_2 are the vertices detected for the areas enclosed by the upward and downward triangles, respectively. The dashed lines represent the minimum values of x-min(x, y, -y), y-min(x, y, -y), and -y-min(x, y, -y) for the areas enclosed by each type of triangle. For example, when the angle of the reference vector is 120° ≤ θ ≤ 240°, (11a) applies; the vertex Q_1 (or Q_2), where y-x and -y-x both reach their minimum, is detected for the upward (or downward) triangle.

Finally, all the available switching states for the vertex (P_2) of the modulation triangle $\Delta P_1P_2P_3$ closest to the origin can be generated as

$$[N+S_a,\ N+S_b,\ N+S_c]^T, \quad \text{where the integer } N \in [0,\ n-1-\max(S_a,S_b,S_c)] \tag{12}$$

where max(S_a, S_b, S_c) is the maximum value among S_a, S_b, and S_c. Since the vertex closer to the origin has more valid switching states (e.g., P_2 has more valid switching states than P_1 and P_3), detecting this vertex leads to the maximum number of switching sequences.

Consider, for example, the reference vector $\boldsymbol{V}_{ref}$ in Fig. 4, which has the value of

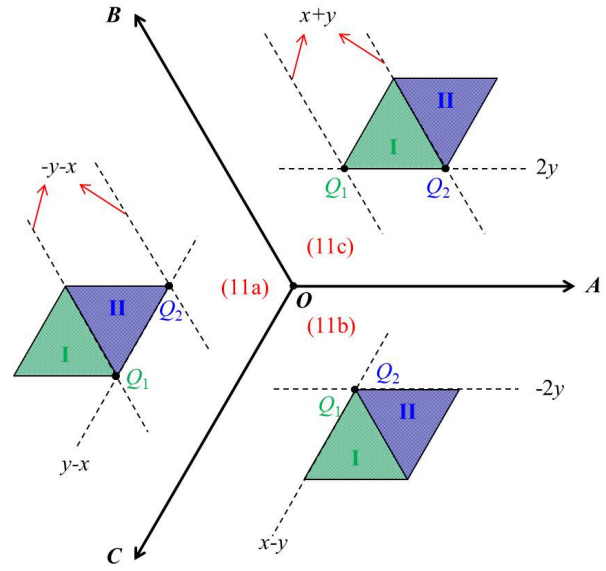

Fig. 7. The vertex detected by (10) for different locations of the reference vector

$$\boldsymbol{V}_{ref} = V_{dc}\cdot(1.55+1.75\cdot j\sqrt{3}) \tag{13}$$

From (4), the real and imaginary coordinates of the reference vector are x=1.55 and y=1.75. Therefore a candidate switching state $S_aS_bS_c$ for P_2 is obtained from (10) as

$$\begin{bmatrix}S_a\\S_b\\S_c\end{bmatrix} = \text{int}\left(\begin{bmatrix}1.55-\min(1.55,1.75,-1.75)\\1.75-\min(1.55,1.75,-1.75)\\-1.75-\min(1.55,1.75,-1.75)\end{bmatrix}\right) = \begin{bmatrix}3\\3\\0\end{bmatrix} \tag{14}$$

In fact, for any reference vector located inside the triangle $\Delta P_1P_2P_3$, min(x, y, -y) = -y since x>0 and y>0, and

$$3 < x+y < 4, \quad 3 < 2y < 4 \tag{15}$$

So wherever the reference vector is located, a candidate switching state 330 will always be generated according to (11c), which means that the vertex (i.e., P_2) of the modulation triangle closest to the origin will always be captured. Eventually, all the available switching states for P_2 are generated by (12), as 441 and 330 shown in Fig. 4. The result can be verified by comparison with the space vector diagram of five-level converters [32].

B. Calculating the Duty Cycles

Once a vertex (closest to the origin O) of the modulation triangle is detected, the origin of the reference vector $\boldsymbol{V}_{ref}$ is shifted to the detected vertex (i.e., P_2 as in Fig. 4), which yields a "remainder vector" $\boldsymbol{V}_{ref}$' as

$$\boldsymbol{V}_{ref}' = \boldsymbol{V}_{ref} - \boldsymbol{OP}_2 \tag{16}$$

where $\boldsymbol{OP}_2$ is obtained by substituting the switching state $S_aS_bS_c$ produced by (10) into (8). Since $\boldsymbol{V}_{ref}$' is inside a two-level hexagon (i.e., H_3 as in Fig. 4) that centers at the detected

TABLE II

ORIGINAL RULE OF DETERMINING SWITCHING SEQUENCES [32]

	reg					
	1	2	3	4	5	6
mode=1	ABC↑(L)	CAB↓(U)	BCA↑(L)	ABC↓(U)	CAB↑(L)	BCA↓(U)
mode=2	CBA↓(U)	BAC↑(L)	ACB↓(U)	CBA↑(L)	BAC↓(U)	ACB↑(L)

TABLE III

SIMPLIFIED MAPPING OF DETERMINING SWITCHING SEQUENCES①②

reg	1	2	3	4	5	6
D_h (h=a, b, or c)	$D_a = 1\text{-}d_{01}$ $D_b = 1\text{-}d_{01}\text{-}d_1$ $D_c = 1\text{-}d_{01}\text{-}d_1\text{-}d_2$	$D_a = d_{01}+d_1$ $D_b = d_{01}+d_1+d_2$ $D_c = d_{01}$	$D_a = 1\text{-}d_{01}\text{-}d_1\text{-}d_2$ $D_b = 1\text{-}d_{01}$ $D_c = 1\text{-}d_{01}\text{-}d_1$	$D_a = d_{01}$ $D_b = d_{01}+d_1$ $D_c = d_{01}+d_1+d_2$	$D_a = 1\text{-}d_{01}\text{-}d_1$ $D_b = 1\text{-}d_{01}\text{-}d_1\text{-}d_2$ $D_c = 1\text{-}d_{01}$	$D_a = d_{01}+d_1+d_2$ $D_b = d_{01}$ $D_c = d_{01}+d_1$

①D_h and 1-D_h are the respective duty cycles of the two switching states K_h+1 and K_h for phase h (h=a, b, or c).

②For both the ascending mode (↑) and descending mode (↓), $K_aK_bK_c$ should not be the top switching state at the detected vertex.

vertex, the duty cycles of the nearest three vectors are determined in the same way as for a two-level SVM, regardless of the level number of the converter.

As shown in Fig. 4, $\boldsymbol{V}_0$, $\boldsymbol{V}_1$, and $\boldsymbol{V}_2$ respectively represent the nearest three vectors $\boldsymbol{OP}_2$, $\boldsymbol{OP}_3$, and $\boldsymbol{OP}_1$ as follows:

$$\boldsymbol{V}_0 = \boldsymbol{OP}_2 - \boldsymbol{OP}_2 = \boldsymbol{0},$$
$$\boldsymbol{V}_1 = \boldsymbol{OP}_3 - \boldsymbol{OP}_2, \quad \boldsymbol{V}_2 = \boldsymbol{OP}_1 - \boldsymbol{OP}_2 \tag{17}$$

The region number *reg* (①-⑥) of the remainder vector $\boldsymbol{V}_{ref}$' in the two-level hexagon H_3 is given [32] by

$$reg = \text{int}(3\theta_{rem}/\pi) + 1 \tag{18}$$

where θ_{rem} ($0 \le \theta_{rem} < 2\pi$) is the angle of the remainder vector with respect to the real axis, and int($3\theta_{rem}/\pi$) represents the integer part of $3\theta_{rem}/\pi$. An alternative way to calculate *reg* is introduced in the Appendix, which avoids the inverse trigonometric computation.

The corresponding duty cycles are then conveniently obtained [32] as

$$\begin{cases} d_1 = \frac{2}{\sqrt{3}}\left[V_{rx}\sin\left(\frac{reg}{3}\pi\right) - V_{ry}\cos\left(\frac{reg}{3}\pi\right)\right] \\ d_2 = -\frac{2}{\sqrt{3}}\left[V_{rx}\sin\left(\frac{reg-1}{3}\pi\right) - V_{ry}\cos\left(\frac{reg-1}{3}\pi\right)\right] \\ d_0 = 1 - d_1 - d_2 \end{cases} \tag{19}$$

where V_{rx} and V_{ry} represent the real and imaginary part of $\boldsymbol{V}_{ref}$'/V_{dc}, respectively; d_1 and d_2 are respectively the duty cycles of $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$; d_0 is the total duty cycle for the "zero vectors", i.e., the switching states at the detected vertex (e.g., 441 and 330 at P_2). This proposed SVM scheme applies two zero vectors (i.e., two redundant switching states) in each switching sequence. The duty cycles d_{01} and d_{02} of the two zero vectors can be freely adjusted [32] as long as

$$d_{02} = d_0 - d_{01}, \quad 0 \le d_{01} \le d_0 \tag{20}$$

Note that no real-time trigonometric calculation is needed for (19), since *reg* only has six integer values (i.e., from one to six). The six possible values of $\sin(\pi \cdot reg/3)$ and $\cos(\pi \cdot reg/3)$ can be pre-calculated.

C. Generating the Switching Sequences

Based on the switching states of the detected nearest vector (e.g., $\boldsymbol{OP}_2$) and the region number *reg* of the remainder vector $\boldsymbol{V}_{ref}$', all the switching sequences can now be generated. There are two switching sequence modes for selection, i.e., *mode*=1 when the switching sequence is counterclockwise (d_{01}*$\boldsymbol{V}_0$→ d_1*$\boldsymbol{V}_1$→ d_2*$\boldsymbol{V}_2$→ d_{02}*$\boldsymbol{V}_0$) as in Fig. 4(b), and *mode*=2 when the switching sequence is clockwise (d_{02}*$\boldsymbol{V}_0$→ d_2*$\boldsymbol{V}_2$→ d_1*$\boldsymbol{V}_1$→ d_{01}*$\boldsymbol{V}_0$) as in Fig. 4(c).

Table II gives a general rule of determining the switching sequences, called the "second mapping" in [32]. The basic principle is that the shifting of vectors can be represented by adjusting the switching states of the corresponding phase. Each element of the mapping includes five sub-elements. The letter A, B, or C means that the switching state of phase *a*, *b*, or *c* is to be modified sequentially in order to switch to another nearest vector. The symbol "↑" or "↓" indicates that the switching state of the corresponding phase is increased or decreased by 1, respectively. For example, if the first switching state (obtained from the detected vertex) of a switching sequence is $S_{a0}S_{b0}S_{c0}$ and the rule is "BAC↑(L)" (i.e., *reg*=2 and *mode*=2), then the switching sequence is generated as $S_{a0}S_{b0}S_{c0}$→ $S_{a0}(S_{b0}+1)S_{c0}$→ $(S_{a0}+1)(S_{b0}+1)S_{c0}$→ $(S_{a0}+1)(S_{b0}+1)(S_{c0}+1)$. As aforementioned, the redundant

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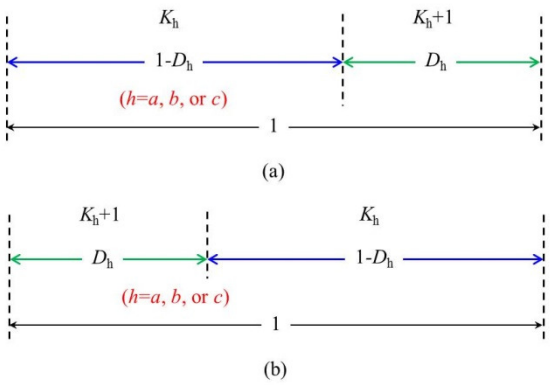


Fig. 8. The two switching sequence modes: (a) ascending mode (↑); (b) descending mode (↓).

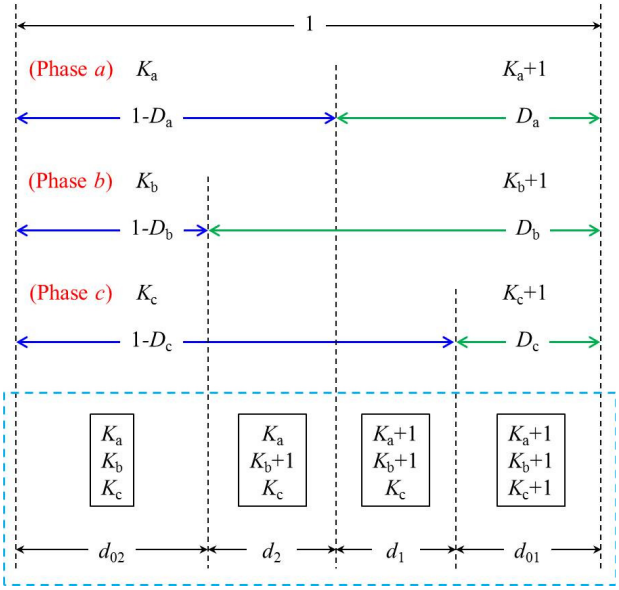


Fig. 9. Equivalence between the two mappings shown in Tables II and III, taking *reg*=2 and *mode*=2 as an example.

switching states at each vertex are listed decreasingly from top to bottom corresponding to the switching states of phase *a*. The letter "L" in the parentheses represents the word "lower" and means that the first switching state $S_{a0}S_{b0}S_{c0}$ should not be the top one at the detected vertex, e.g., not 441 for vertex P_2; the letter "U" in the parentheses represents the word "upper" and means that the first switching state $S_{a0}S_{b0}S_{c0}$ should not be the bottom one at the detected vertex, e.g., not 330 for vertex P_2. Accordingly, the switching sequences for the reference vector $\boldsymbol{V}_{ref}$ in Fig. 4 are generated as 441 → 440 → 340 → 330 (*mode*=1) and 330 → 340 → 440 → 441 (*mode*=2), as shown in Figs. 4(b) and (c).

Though the mapping in Table II generates all the optimized switching sequences [24] [32] [33] (with the minimum number of switch transitions in every switching cycle) for any multilevel converter and reference vector, its implementation is still relatively more complicated than the phase-voltage modulation techniques (carrier-based modulation and nearest-level modulation), because of the encoding (which causes complexity and extra memory consumption in real-time

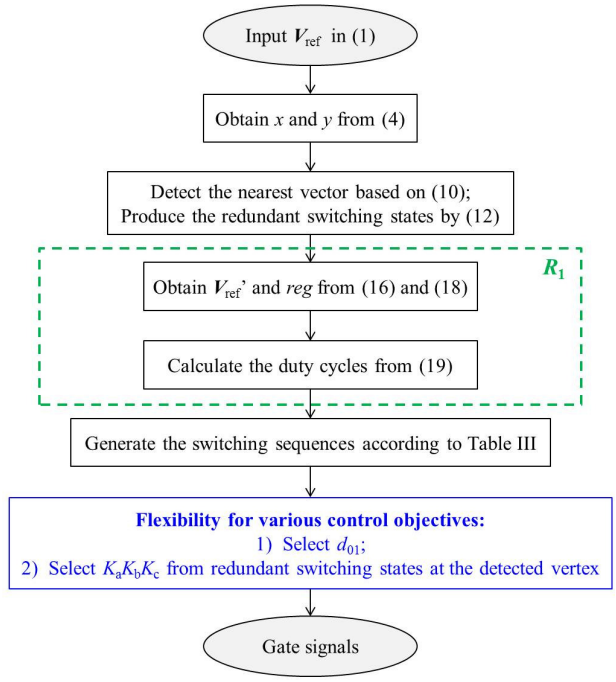
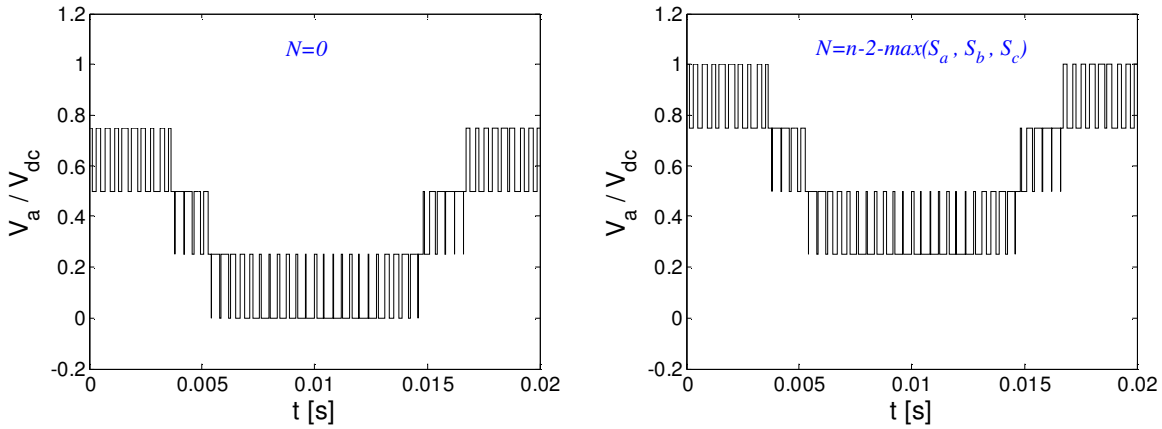


Fig. 10. Flowchart for the proposed SVM scheme

implementation) needed for the four switching states and the respective duty cycles in each switching sequence. An earlier work has demonstrated that SVM and nearest-level modulation produce identical switching sequences, despite their apparent differences [24]. However, is it possible to simplify the generation of switching sequences for SVM based on the concept of nearest-level modulation? A further simplified mapping summarized in Table III answers this question, as explained later.

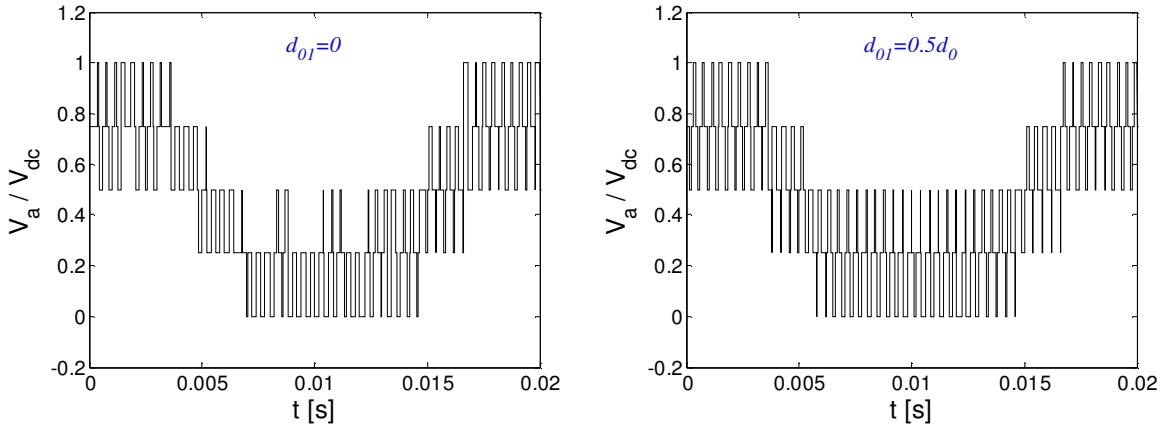
At first, it is observed from Table II that for the switching state of phase *h* (*h*=*a*, *b*, or *c*), there are only two successive values K_h and K_h+1 in each optimized switching sequence [24] [32]; $K_aK_bK_c$ and $(K_a+1)(K_b+1)(K_c+1)$ are the two "zero vectors". Fig. 8 shows the switching state of each phase according to the "↑" and "↓" switching sequence modes (called the ascending mode and descending mode, respectively) in Table II. As demonstrated in [24], if the respective duty cycles of K_h and K_h+1 (i.e., 1-D_h and D_h) are equal to that of the switching sequence produced by Table II, then the same switching sequence is equivalently achieved in Fig. 8. For example, when *reg*=2 and *mode*=2, the four switching states and the corresponding duty cycles in the switching sequence are $d_{02}{*}S_{a0}S_{b0}S_{c0} \rightarrow d_2{*}S_{a0}(S_{b0}+1)S_{c0} \rightarrow d_1{*}(S_{a0}+1)(S_{b0}+1)S_{c0} \rightarrow d_{01}{*}(S_{a0}+1)(S_{b0}+1)(S_{c0}+1)$ according to Table II. The same sequence is therefore equivalently achieved in Fig. 8(a) if $K_h=S_{h0}$ and D_h is the value shown in Table III (*reg*=2), as demonstrated in Fig. 9. Finally, Table III lists the results for all the other cases. The discontinuous SVM patterns [33] (i.e., eliminating either the first or last switching state in each sequence) can be easily achieved by setting d_{01}=0 or $d_{01}=d_0$.

Note that when using Table III, $K_aK_bK_c$ should not be the top switching state at the detected vertex, for both the



(a) (b)

Fig. 11. Simulated phase *a* voltage (with respect to the negative terminal of the dc-link) according to different switching states selected for the detected vertex, when $d_{01}=0.5d_0$: (a) $K_aK_bK_c$ is the bottom switching state; (b) $K_aK_bK_c$ is the second top switching state



(a) (b)

Fig. 12. Simulated phase *a* voltage (with respect to the negative terminal of the dc-link) according to different d_{01}: (a) $d_{01}=0$; (b) $d_{01}=0.5d_0$

ascending (↑) and descending (↓) modes in Fig. 8. This is easily understood because otherwise K_h+1 ($h=a$, b, or c) exceeds $n-1$.

D. Summary

Fig. 10 gives the overall flowchart of the proposed SVM scheme. Because of the proposed mapping (Table III), the encoding (for the switching states of the nearest three vectors and the respective duty cycles in each switching sequence) required by earlier SVM methods is avoided. The switching sequences are easily generated by controlling the duty cycle of each phase, which is the same procedure as for the nearest-level modulation method. Therefore, considering the extra flexibility (i.e., redundant switching states and adjustable duty cycles), the proposed scheme is more advanced than the phase-voltage modulation techniques (carrier-based modulation and nearest-level modulation), even for large level-number applications.

The switching state $K_aK_bK_c$ and the duty cycle d_{01} can be selected according to different control objectives, such as the best harmonic performance [33] [39] or the optimal capacitor voltage balancing [40] [41]. Because of the proposed mapping (Table III), any achieved control objective is accompanied by the optimized switching sequences [24] [32] [33] (with the minimum number of switch transitions in every switching cycle). This feature leads to reduced switching losses and dv/dt, especially when the level number of the converter is large.

To avoid cross conduction during switch transitions, dead times can be added when generating the gate signals, through control software (modifying the duty cycles in Table III) or gate driver hardware. Meanwhile, many compensation methods [42]-[47] can reduce voltage errors caused by the dead times and non-ideal characteristics of switching devices.

The proposed new scheme can potentially be extended to simplify the SVM for multiphase multilevel converters [37], based on the orthogonal unit-vectors introduced in Section II. In multiphase applications, more redundant switching states exist [38]. A simplified scheme implies significantly reduced costs of implementation. As demonstrated in this paper for the three-phase converters, the final objective is to implement the multiphase multilevel SVM in the same way as for the phase-

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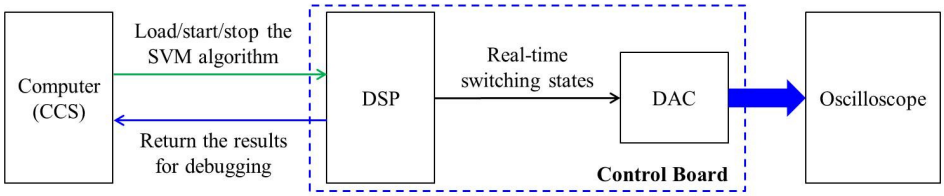
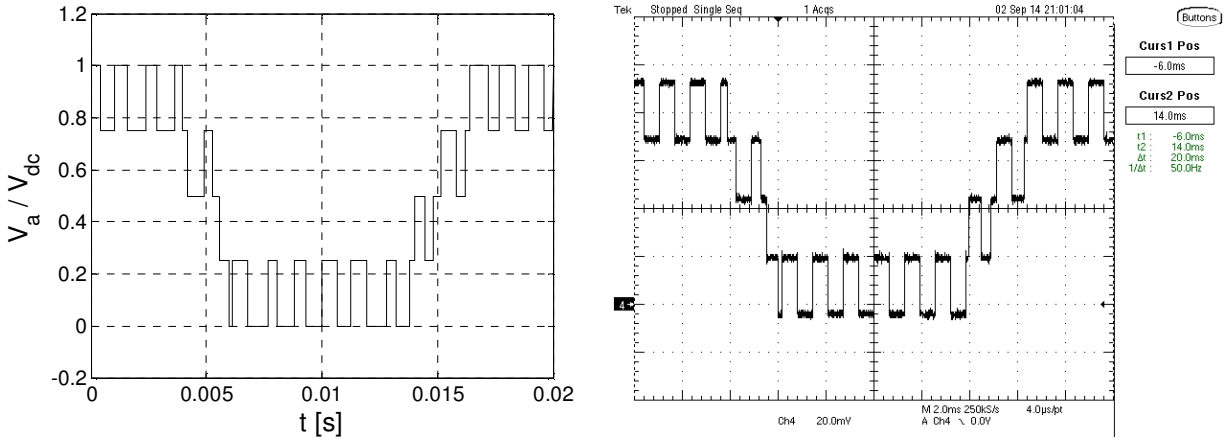


Fig. 13. Schematic diagram of the experimental setup



(a) (b)

Fig. 14. Simulation and experimental results of the phase voltage (phase *a*) for a five-level converter: (a) simulated in MATLAB/Simulink; (b) measured from the DAC output, represented by the corresponding switching states generated by the proposed SVM scheme on the DSP

voltage modulation techniques, while maintaining significant flexibility.

IV. Simulation and Experimental Results

A. Simulation Results

To demonstrate the two degrees of freedom (i.e., the redundant switching sequences and the adjustable duty cycles) of the proposed new scheme, a simulation is implemented in MATLAB/Simulink for a three-phase five-level converter. In the simulation, the switching frequency is 5 kHz (fundamental frequency is 50 Hz), the modulation index is 0.6 (i.e., a low-modulation region in order to produce redundant switching states), and the switching sequence mode is changed (alternately from the ascending mode to the descending mode) after every switching cycle.

Fig. 11 shows the simulated output voltage of phase *a* when d_{01}=0.5d_0, according to different redundant switching sequences. In Fig. 11(a), $K_aK_bK_c$ is directly the switching state detected in (10). In other words, it is the bottom switching state at the detected vertex, by letting N=0 in (12). Fig. 11(b) selects $K_aK_bK_c$ as the second top switching state at the detected vertex, i.e., N=n-2-max(S_a, S_b, S_c). Since different selections of $K_aK_bK_c$ lead to varied switching waveforms as in Fig. 11, the proposed new scheme offers significant potential for optimizing the performance of a multilevel converter.

Fig. 12 illustrates the other degree of freedom (i.e., flexible d_{01}) provided by the proposed new scheme. To represent all the possible switching states of phase *a*, $K_aK_bK_c$ is intentionally selected as the second top switching state at the detected vertex for the ascending mode, and as the bottom switching state for the descending mode. The waveform in Fig. 12(a) is the voltage of phase *a* when d_{01}=0, which actually displays a discontinuous SVM pattern. It is significantly different from the voltage of phase *a* shown in Fig. 12(b), where the duty cycles of the two zero vectors are equal (i.e., d_{01}=0.5d_0). Again, the varied switching waveforms indicate more potential for improving the performance of multilevel converters.

B. Experimental Results

In order to verify the real-time implementation of the proposed new scheme, an experiment is carried out on a TMS320CF2812 digital signal processor (DSP). Fig. 13 presents the schematic diagram of the experimental setup. The experiment is implemented by running the proposed SVM algorithm on the DSP in real time for any reference vector of a three-phase five-level converter. The Code Composer Studio (CCS) [48] on a computer, which loads the compiled SVM algorithm to the DSP and starts or stops the execution of the algorithm on the DSP as needed, is applied to interface with the DSP. The DSP does not actually drive any power electronic switches, but instead sends the switching states generated by the proposed scheme to a digital-to-analog converter (DAC), which represent the phase voltages of the five-level converter as described in (8). An actual five-level converter is not required. Finally, the DAC output is measured by an oscilloscope.

The switching frequency is 1.3 kHz (fundamental frequency is 50 Hz) for the experiment, in order to highlight the switch

transitions. Other operating conditions are as follows. The modulation index is 0.9 (in order to display all the voltage levels); the duty cycles of the two zero vectors are equal (i.e., d_{01}=0.5d_0); and the switching sequence mode is changed (alternately from the ascending mode to the descending mode) after every switching cycle. Fig. 14(a) shows the simulated voltage of phase *a* (relative to the negative terminal of the dc-link) in MATLAB/Simulink for the same operating conditions. The experimental result measured from the DAC output is demonstrated in Fig. 14(b), which is consistent with the simulation result and therefore validates the real-time implementation of the proposed new scheme.

C. Comparison of Real-Time Implementation

In the previous sections, some advantages of the proposed new scheme (e.g., the simplified generation of switching sequences, and the potential for multiphase multilevel applications) have been described in detail. This section further demonstrates another advantage (i.e., the superior computational efficiency), by comparing the proposed new scheme with the two typical methods introduced in [27] and [32]. Other SVM methods can be analyzed in a similar way. In the Appendix, a supplementary explanation of the methods in [27] and [32] is presented.

Based on the experimental setup in Fig. 13, the computational times of the three SVM schemes (the proposed new scheme, the scheme in [27], and the scheme in [32]) on the DSP are compared. Table III is applied to generate the switching sequences for all the three schemes, since no method of generating the switching sequences is given in [27] and the mapping (Table II) introduced in [32] is significantly simplified in the proposed new scheme (Table III). In addition, the scheme in [27] is further simplified by applying the concept proposed in this paper, e.g., (25) and (27) in the Appendix. The modulation index is 0.9; the duty cycles of the two zero vectors are equal (i.e., d_{01}=0.5d_0); and the switching sequence mode is changed (alternately from the ascending mode to the descending mode) after every switching cycle. Since the proposed new scheme and the method in [27] are independent of the level number (*n*) of the converter, only the result when *n*=5 is presented for these two schemes. On the other hand, the scheme in [32] is evaluated when *n*=5 and *n*=10.

The results in Fig. 15 demonstrate that the proposed new scheme is computationally significantly more efficient than the method in [32], and is slightly more efficient than the method in [27]. However, compared to the method in [27], the proposed new scheme is more attractive because of the simplified rule of generating switching sequences (Table III) and the potential for multiphase multilevel applications.

V. Conclusion

This paper proposes a simplified space vector modulation (SVM) scheme, for any three-phase multilevel converter. Based on two orthogonal unit-vectors that decouple the three-phase components, the proposed scheme is independent of the level number of the converter. Simulation and experimental results verify this new concept.

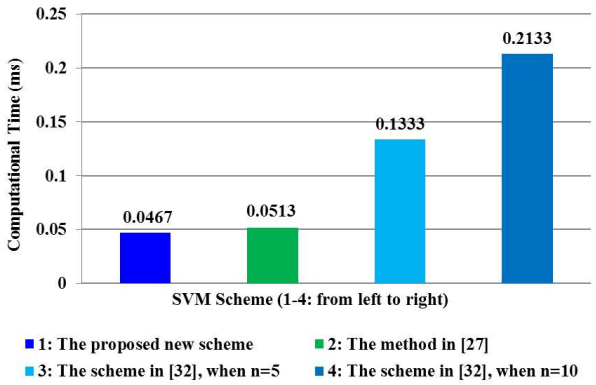


Fig. 15. Computational times of the three SVM schemes (the proposed new scheme, the scheme in [27], and the scheme in [32]) on the DSP

The proposed scheme is computationally extremely efficient. It achieves the same easy implementation as the phase-voltage modulation techniques, while maintaining the significant flexibility (i.e., redundant switching sequences and adjustable duty cycles) for optimizing the switching patterns. Therefore, it is well suited to large level-number applications. Compared with earlier SVM methods, the proposed scheme significantly simplifies the detection of the nearest three vectors and the generation of switching sequences. No lookup table or coordinate transformation is required.

This paper also introduces a general approach to construct the orthogonal unit-vectors for any other multiphase system. Therefore, the proposed scheme can potentially be extended to simplify the SVM for multiphase multilevel converters.

Appendix

A. An Alternative Way to Detect the Nearest Three Vectors

Similar to (10), the candidate switching states for the other two nearest vectors can also be directly obtained as follows

$$\begin{bmatrix} S_{a2} \\ S_{b2} \\ S_{c2} \end{bmatrix} = \text{int}\left(\begin{bmatrix} x - \text{mid}(x, y, -y) \\ y - \text{mid}(x, y, -y) \\ -y - \text{mid}(x, y, -y) \end{bmatrix} \right) \tag{21a}$$

$$\begin{bmatrix} S_{a3} \\ S_{b3} \\ S_{c3} \end{bmatrix} = \text{int}\left(\begin{bmatrix} x - \max(x, y, -y) \\ y - \max(x, y, -y) \\ -y - \max(x, y, -y) \end{bmatrix} \right) \tag{21b}$$

where mid(x, y, -y) and max(x, y, -y) respectively mean the middle and maximum values among x, y, and -y; int(γ) rounds the elements of γ to the nearest integers towards minus infinity. The explanation of (21) is similar to the demonstration in (11) and Figs. 6 and 7. Correspondingly, (21b) detects the vertex of the modulation triangle that is farthest from the origin of the space vector diagram.

For any candidate switching state $S_aS_bS_c$ given by (21), all the available switching states of the detected nearest vector can be generated [32] as

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$$[N+S_a, N+S_b, N+S_c]^T, \quad \text{where the integer } N \in [-\min(S_a,S_b,S_c),\ n-1-\max(S_a,S_b,S_c)] \tag{22}$$

B. An Alternative Way to Calculate reg

The region number, *reg*, of the remainder vector $\boldsymbol{V}_{\text{ref}}'$ in (18) can also be calculated as

$$reg = \begin{cases} 1, & \textbf{if } (0 \le V_{ry} < \sqrt{3}V_{rx}); \\ 2, & \textbf{else if } (V_{ry} \ge \sqrt{3}V_{rx} \textbf{ and } V_{ry} > -\sqrt{3}V_{rx}); \\ 3, & \textbf{else if } (0 < V_{ry} \le -\sqrt{3}V_{rx}); \\ 4, & \textbf{else if } (\sqrt{3}V_{rx} < V_{ry} \le 0); \\ 5, & \textbf{else if } (V_{ry} \le \sqrt{3}V_{rx} \textbf{ and } V_{ry} < -\sqrt{3}V_{rx}); \\ 6, & \textbf{else}. \end{cases} \tag{23}$$

where V_{rx} and V_{ry} represent the real and imaginary part of $\boldsymbol{V}_{\text{ref}}'/V_{\text{dc}}$, respectively.

C. Comparison with Earlier Methods

The flowchart of the SVM method in [27] is illustrated in Fig. 16, which is found by an anonymous reviewer with reference to Fig. 7 and (10). The required equations are

$$g = \frac{V_{ref(x)} - V_{ref(y)}/\sqrt{3}}{V_{dc}}, \quad h = \frac{2V_{ref(y)}}{\sqrt{3}V_{dc}} \tag{24}$$

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \text{int}\left(\begin{bmatrix} g - \min(g,0,-h) \\ 0 - \min(g,0,-h) \\ -h - \min(g,0,-h) \end{bmatrix} \right) \tag{25}$$

$$sgn = g + h - \text{ceil}(g) - \text{floor}(h) \tag{26}$$

$$s = \begin{cases} 1, & \textbf{if } (h > 0 \textbf{ and } h \ge -g); \\ 2, & \textbf{else if } (h \le 0 \textbf{ and } g > 0); \\ 3, & \textbf{else}. \end{cases} \tag{27}$$

where g and h are the coordinates of $\boldsymbol{V}_{\text{ref}}$ in the 60° coordinate system; (25) is a representation of (10) in the 60° coordinate system; ceil(g) rounds g to the nearest integer towards infinity; floor(h) rounds h to the nearest integer towards minus infinity; s indicates the three different locations of the reference vector according to Fig. 7. The duty cycles d_{ll}, d_{ul}, d_{lu}, and d_{uu} are defined in [27]. Note that the operation encircled by the dashed rectangle R_2 in the flowchart is easily achieved by (16), (18), and (19) in the proposed new scheme, as highlighted by the dashed rectangle R_1 in Fig. 10.

Fig. 17 shows the detection of the nearest vector for the SVM method in [32], which requires the following steps:

1) Determines the initial virtual level number n_0, or the hexagon (H_0) that encloses the original reference vector;
2) Detects the n_0-1 level hexagon (H_1) that contains the reference vector, and updates n_0 to n_0-1;
3) Shifts the origin (O) of the reference vector to the center vertex (O_1) of the detected hexagon, which yields a new reference vector;

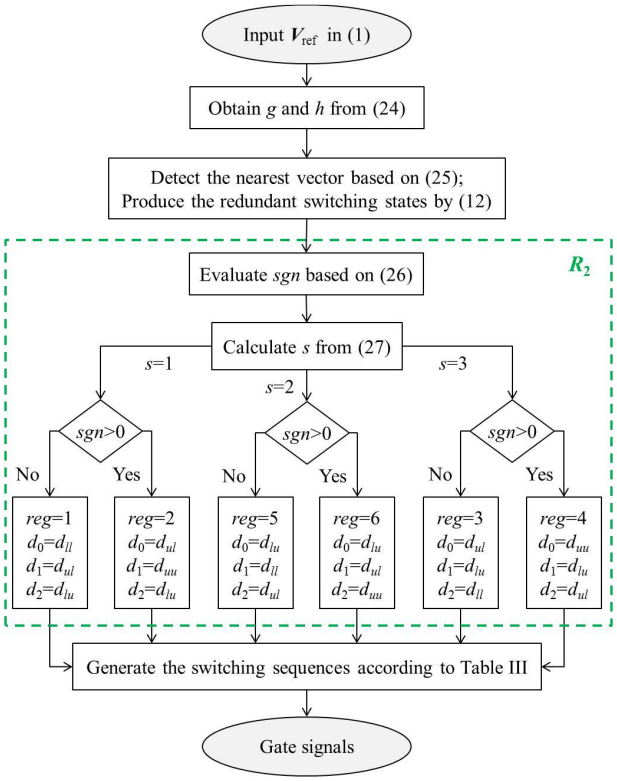

Fig. 16. Flowchart for the SVM scheme in [27]

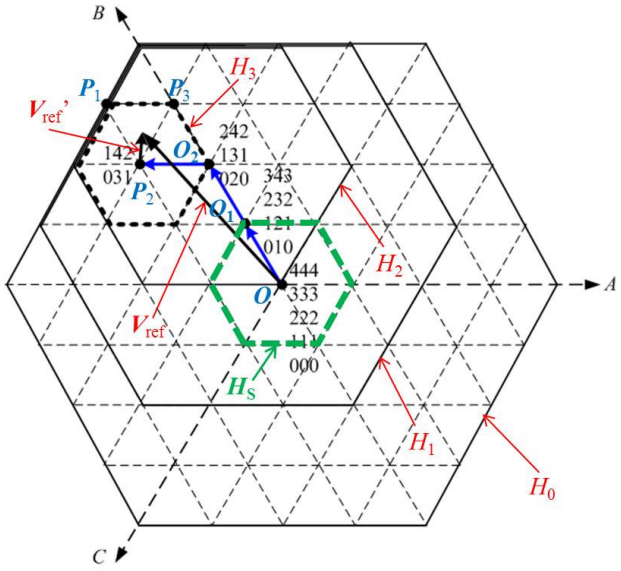

Fig. 17. Nearest vector detection of the SVM scheme in [32]

4) Calculates the switching state for the center vertex (O_1) of the detected hexagon, based on the shifting ($\boldsymbol{OO}_1$) of the reference vector;
5) Repeats the steps 2) - 4) for the new reference vector, until a two-level hexagon (H_3) that encircles the vertex of the original reference vector is found.

This procedure depends on the level number of the converter and the location of the reference vector, and requires iterative calculations. These iterative calculations lead to extra computational effort, but are simply replaced by (10) in the

proposed new scheme. Therefore, the proposed new scheme is faster than the method in [32] in most cases, i.e., when the reference vector is located outside the innermost two-level hexagon (the hexagon H_S shown in Fig. 17). The computational burdens of the method in [32] and the proposed new scheme are equivalent only when the reference vector is enclosed by the innermost two-level hexagon H_S.

ACKNOWLEDGMENT

Y. Deng would like to thank the Mitsubishi Electric Research Laboratories (MERL), Cambridge, MA for their support, as a part of the work was done at MERL when he was a research intern.

The authors would like to thank the anonymous reviewers and editors for their constructive comments.

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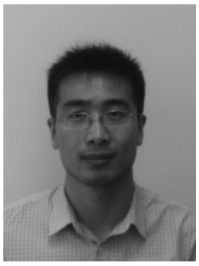

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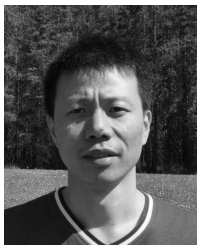

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