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TR2018-075 July 12, 2018

Abstract

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IEEE International Microwave Symposium (IMS)

An FPGA-based Multi-level All-Digital Transmitter with 1.25 GHz of Bandwidth

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***Abstract*—This paper presents the first real-time Field-Programmable Gate Array (FPGA)-based All-Digital Transmitter architecture with a usable bandwidth of 1.25 GHz. The proposed architecture was implemented and embedded into an FPGA, and the results surpass the reported state-of-the-art. Measurement results in terms of Signal-to-Noise Ratio (SNR) and Error-Vector Magnitude (EVM) are presented and discussed. Specifically, modulated signals of 1.25 GHz of bandwidth were successfully transmitted with 30.51 dB of SNR and 2.23% of EVM.**

***Index Terms*—FPGA-based Transmitters, All-Digital RF Transmitters, Delta-Sigma Modulators**

I. Introduction

The demanding requirements of the communication systems have induced an increasing digital-centric design of RF transceivers. All-Digital Transmitters (ADTs) propose a digital datapath from baseband up to the RF stage with a low number of output levels. They enable the design of reconfigurable, agile, multi-standard, and multi-band RF transmitters.

Even though the promising architectures that have been proposed in the State-of-the-Art (SoA), the transmission Bandwidth (BW) is quite limited. To overcome this, the use of parallel Delta-Sigma Modulators ($\Delta\Sigma$Ms) was proposed in [1], leading to the usable BW of 125 MHz. Then, an optimized 2nd-order Time-Interleaved $\Delta\Sigma$M with 488 MHz of BW was also reported in [2]. However, in all the typical SoA works, the application of the Digital Up-Conversion (DUC) after the pulse encoding requires challenging serializer sampling rates (e.g. 20 and 60 Gbps in [2], [3], respectively). Nonetheless, in addition to the increased complexity and cost, the design of analog front-ends becomes quite challenging. Thus, this paper presents a novel architecture capable of transmitting BWs up to 1.25 GHz, embedded into a Field-Programmable Gate Array (FPGA), with a serializer bitrate of 10 Gbps. The carrier frequency is 2.5 GHz, but the same architecture can be synthesized to operate at any other carrier frequency ($<$ 5 GHz), with minor updates in the implemented hardware.

The remainder of this paper is organized as follows. In the next section, the parallel $\Delta\Sigma$M based architecture is presented. Section III presents the FPGA-based ADT transmitter architecture. Section IV shows the experimental results. The conclusions are drawn in Section V.

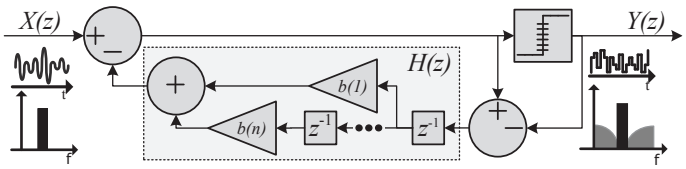

Fig. 1: Representation in z-domain of an Error-Feedback $\Delta\Sigma$M with Finite Impulse Response (FIR) feedback loop.

II. Main Architecture

A. RF-stage $\Delta\Sigma$M with Propagation of State Registers

To achieve a high sampling rate in the Pulse Encoder, the multicore $\Delta\Sigma$M based on propagation of state registers (reported in [4]) was selected and implemented. This architecture achieves high sampling rates by feeding *N* independent slices (of size *K*) from the same input signal to *N* $\Delta\Sigma$Ms. In addition to that, input/output samples from the $\Delta\Sigma$Ms are delayed to ensure a propagation of the state-registers between adjacent modulators. To relax the bitrate requirements, the DUC was applied before the Pulse Encoder (following the concept of RF-stage $\Delta\Sigma$Ms proposed in [5]), leading to sampling rates in the Pulse Encoder equal to the serializer's sampling rate.

B. Delta-Sigma Modulator Design

The design of the Delta-Sigma ($\Delta\Sigma$) modulator must be done according to the required notch BW. However, at the same time, the critical path must be as short as possible, reason for why such architectures as Cascade-of-Resonators, FeedBack/FeedForward (CRFB/F) or Cascaded-of-Integrators, FeedBack/FeedForward (CIFB/F) are not suitable. Thus, the generic Error-Feedback (EF) $\Delta\Sigma$ architecture with a FIR feedback loop (depicted in Fig. 1) was selected as a starting point. This architecture was derived from the conventional 2nd-order EF-$\Delta\Sigma$M, by adding two complex zeros per required notch. For the sake of simplicity, let us restrain the number of notches to 3. By modeling the quantization noise by a random noise signal:

$$\begin{aligned} NTF(z) &= \left(1+\alpha z^{-1}+z^{-2}\right).\left(1+\beta z^{-1}+z^{-2}\right). \\ &\quad .\left(1+\gamma z^{-1}+z^{-2}\right) \end{aligned} \tag{1}$$

where α, β and γ are defined as $-2\cos\left(2\pi Fc/Fs\right)$, Fs is the sampling frequency, and Fc is the required notch frequency.

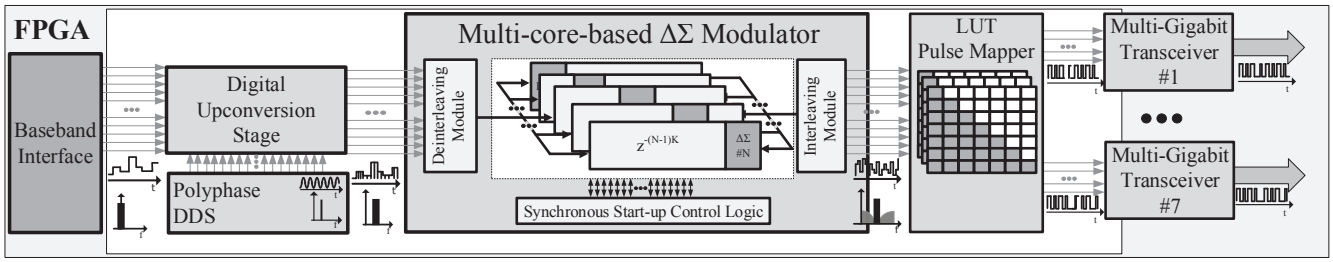

Fig. 2: General block diagram of the implemented All-Digital RF Transmitter, embedded into an FPGA.

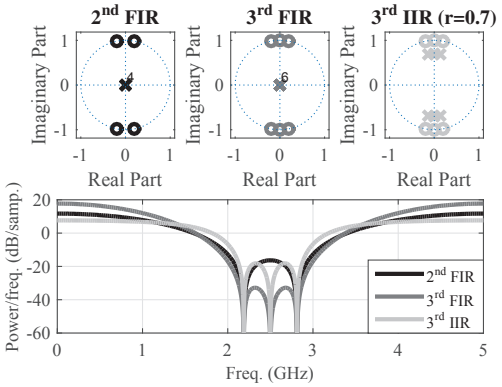

Fig. 3: Noise-Transfer Function (NTF)'s frequency response and zero-poles placement according to the different feedback-loop transfer functions.

As $NTF(z) = 1 + H(z)$, where $H(z)$ is the feedback loop transfer function, $H(z)$ can be computed as:

$$H(z) = b(1)z^{-1} + b(2)z^{-2} + b(3)z^{-3} + b(4)z^{-4} + \\ + b(5)z^{-5} + b(6)z^{-6} \quad (2)$$

where $b(1) = (\alpha + \beta + \gamma)$, $b(2) = (3 + \alpha\beta + \gamma(\alpha + \beta))$, $b(3) = (2(\alpha + \beta) + \gamma(2 + \alpha\beta))$, $b(4) = (3 + \alpha\beta + \gamma(\alpha + \beta))$, $b(5) = (\alpha + \beta + \gamma)$, and $b(6) = 1$. After deriving the coefficients, simulations were carried out in Matlab to choose the order of the feedback loop suitable to achieve around 1.25 GHz of usable bandwidth (Fig. 3). The notches were uniformly distributed into the desired bandwidth. While comparing the 2nd and 3rd FIR curves, it can be realized that the latter is the only that fulfills the specification with better performance. However, the typical wireless modulated signals (briefly specified in terms of Peak-to-Average Power Ratio (PAPR), order of the modulation, and bandwidth) preclude the implementation of this architecture with a single-bit output, due to stability issues. While the SoA proposes the inclusion of poles to ensure the stability, it is also depicted in Fig. 3, that their inclusion reduces the achievable bandwidth. Thus, our solution passes through the use of more bits in the output (in particular 8 levels were used for the sake of proof-of-concept).

III. FPGA-based All-Digital RF Transmitter Architecture

The block diagram of the implemented ADT is depicted in Fig. 2. The baseband data is interpolated to the serializer's sampling rate, divided into 64 phases and forwarded to the polyphase DUC. This division into *N* phases is always required, due to the limited sampling rate from the FPGA programmable logic subsystems, that is far below the bandwidth of the input signal (typically less than 300 MHz). Each phase is clocked at Fs_{BB}, providing an equivalent sampling rate of $Fs_{MGT} = NFs_{BB}$. The DUC is composed of a polyphase Digital Direct Synthesis (DDS), working as Local Oscillator (LO). The carrier frequency was chosen to be 2.5 GHz. The resultant data is forwarded to a De-interleaving module, that temporarily stores and re-arranges the data into *N* blocks of size *K*. These blocks feed the *N* phases to the Multi-core 8-level $\Delta\Sigma$ architecture. The computed encoded equivalents are temporarily stored and re-arranged again by the Interleaving Module. It must be pointed out that the "Synchronous Start-up Control Logic" was included to ensure the propagation of the state-registers as presented in [4]. This enables a reduction of K while maintaining a given performance. Ultimately, the latency is improved, as well as the memory resources usage. Moreover, in this work, we forced K to be equal to N, in order to replace the First-In First-Outs (FIFOs) (proposed by the authors to be used in the Deinterleaving/Interleaving modules [4], [5]) by just registers and multiplexers. Afterwards, a Look-Up Table (LUT)-based mapper encodes the 3-bit samples into 7 single-bit streams, that will be serialized by 7 MGTs.

IV. Experimental Results

To validate the proposed approach, an ADT was fully implemented into a Virtex Ultrascale XCVU095 FPGA using the Xilinx VCU1287 Characterization Kit. The Multi-Gigabit Transceivers (MGTs)' sampling rate were configured to 10 Gbps, and lane-to-lane deskew techniques were implemented. The experimental setup is depicted in Fig. 4. Due to the challenges of measuring the 7 MGT channels at the same time, an extra MGT was included as an embedded trigger in the acquisition of all the channels with a 4-port Real-time Oscilloscope (Keysight DSA-X 92504Q). The Tektronix AWG610 generates the FPGA reference clock and forwards a 10 MHz reference to the oscilloscope. After having all the channels acquired, the 7 streams are simply combined (note

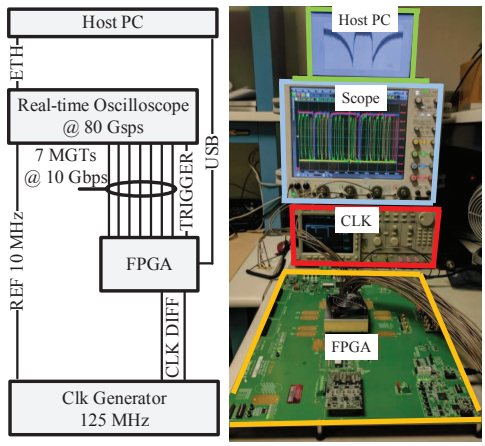

Fig. 4: Block diagram and photo of the experimental setup.

that no post-processing, such as timing/amplitude corrections, is applied) and the signal analysis and demodulation is done through the LabView VSA Software from National Instruments. Experimental results were obtained and, in particular, spectrum and Error-Vector Magnitude (EVM) measurements are reported.

The comparison between the simulated and the measured 16-Quadrature Amplitude Modulation (QAM) modulated signal with 1.25 GHz (symbol rate of 1 Gsps and RRC of 0.25) is demonstrated in Fig. 5 a). It can be observed the good agreement between both data. The performance drop in terms of Signal-to-Noise Ratio (SNR) (also observed in the same figure) is resultant from the amplitude mismatch between the different MGTs. Different measured spectra and respective constellations for bandwidths of 312.5 MHz, 625 MHz and 1.25 GHz are presented in Fig. 5 b). These measurements were obtained from three different hardware implementations, with a uniform placement of the three notches to cover the required bandwidth.

Table I (a) summarizes the obtained EVM-SNR pairs obtained for the different BWs. All the experimental results present EVM values below 2.5%, even for the case of 1.25 GHz of bandwidth, attesting the validity of the proposed architecture. Moreover, to the best of author's knowledge, this is the maximum bandwidth ever reached with an FPGA-based ADT architecture (the maximum value of 488 MHz was previously reported in [2]). The occupied resources are depicted in Table I (b). It should be mentioned that the Block Random-Access Memory (BRAM) primitive could be used to balance the high utilization of the Memory LUT.

All the experimental results attest the validity of the proposed architecture. For the sake of this proof-of-concept, the assessment of the outputs was done with a high-speed oscilloscope. However, the promising results in terms of signal integrity anticipate that analog combining networks can be incorporated. The envisioned combination network is based on the asymmetric extended H-bridge [6], [7] and its design should be done in order to maximize the performance in the combination of multiple Switched-Mode Power Amplifiers

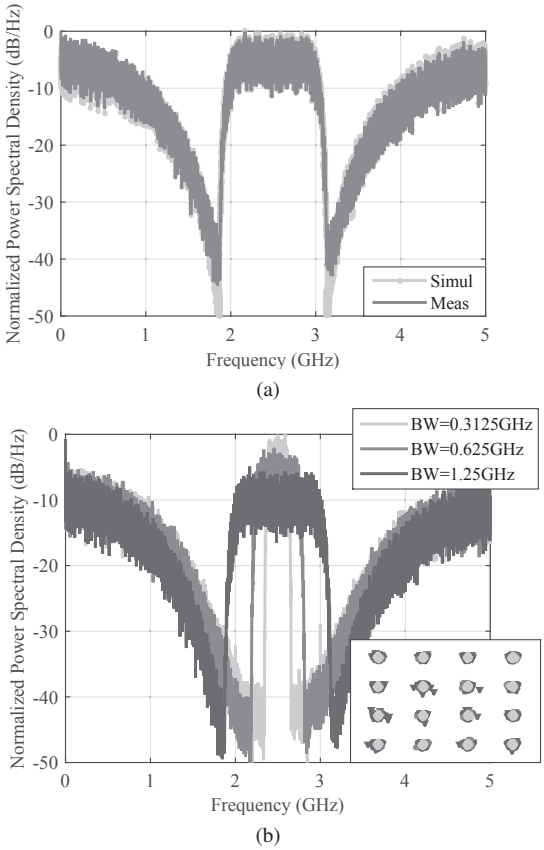

Fig. 5: (a) Comparison of the simulated and measured spectra with a 16-QAM modulated signal with 1.25 GHz; (b) Different measured spectra and respective constellations with BWs of 312.5 MHz, 625 MHz and 1.25 GHz.

TABLE I

(a) SNR/EVM pairs for a 16-QAM signal. BW is in GHz, EVM in % and SNR in dB. (b) Resources usage of the proposed architecture

(a)

BW	SNR	EVM
0.3125	36.90	1.05
0.625	36.58	1.10
1.25	30.51	2.23

(b)

Resources	Used	Total	%
Flip Flops	35411	1075200	3.3
LUTs	94627	537600	17.6
Mem. LUT	57882	76800	75.3
BRAM	0	1728	0
DSP48	128	768	16.6
GTHs	8	28	28.5

(SMPAs). Following our proposed architecture, the analog impairments (in terms of phase imbalances, or magnitude mismatches) can be easily compensated in the digital domain. Thus, the most stringent requirement, from a designer point-of-view, is the synchronization between multiple lanes that must be ensured.

V. Conclusion

In this paper, a new architecture capable of achieving 1.25 GHz of bandwidth is proposed. The technique was implemented and validated into an FPGA-based ADT. In addition to achieve a superior performance in terms of wideband

capability, the fully digital behavior of this architecture shows a strong potential to be synthesized in custom application specific integrated circuits. Work in the design of an efficient power combining network is on the way, so that a complete multi-level ADT system can be demonstrated.

VI. Acknowledgement

This work is supported by Mitsubishi Electric Research Laboratories. With additional support for Daniel C. Dinis, Arnaldo S. R. Oliveira and José Vieira provided by FCT/MEC through national funds and when applicable co-funded by FEDER PT2020 partnership agreement under the project UID/EEA/50008/2013, by the European Regional Development Fund (FEDER), through the Competitiveness and Internationalization Operational Programme (COMPETE 2020) of the Portugal 2020 framework, Project RETIOT, POCI-01-0145-FEDER-016432, and by FCT - Fundação para a Ciência e a Tecnologia - under the PhD (PD/BD/105857/2014) grant given to the first author.

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