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Abstract

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A Real-time Architecture for Agile and FPGA-based Concurrent Triple-Band All-Digital RF Transmission

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***Abstract*—Contiguous/Non-Contiguous Carrier Aggregation (CA) is one of the key features from 4G systems that is expected to be evolved within 5G technologies. Thus, there is a need for the development of flexible, agile and reconfigurable radio transceivers with a native support for the integration of multiple bands and multiple standards. All-Digital RF Transmitters have demonstrated promising potential to the design of next-generation RF transceivers. However, the simultaneous multi-band transmission is still one of the key limitations of current approaches. To address this problem, this paper presents a fully digital and parallel architecture that enables the real-time design of agile and concurrent triple-band transmission. The proposed architecture is suitable for both Contiguous and Non-Contiguous CA scenarios, and considerably surpasses the state-of-the-art in terms of frequency agility, maximum spacing between bands, and aggregated bandwidth. To enhance the system performance, an extension to a multi-level architecture, based on the analog combination of pulsed waveforms, is also demonstrated. Both architectures (2- and 7-level) were implemented in a Field-Programmable Gate Array (FPGA). Measurement results in terms of Signal-to-Noise Ratio (SNR), Error-Vector Magnitude (EVM) and Adjacent-Channel Power Ratio (ACPR) are presented and discussed. Implementation-I, the 2-level architecture presents a frequency agility from 0.1 to 2.5 GHz (with a frequency resolution of 4.88 MHz) with an aggregated bandwidth of 56.26 MHz. Implementation-II, the 7-level design presents a frequency agility from 0.1 to 2 GHz (with a frequency resolution of 3.906 MHz) with an aggregated bandwidth of 112.5 MHz.**

***Index Terms*—ALL-Digital Transmitters, carrier aggregation, delta-sigma modulation, field-programmable gate array (FPGA)-based transmitters, multi-band RF transmission, software-defined radio.**

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I. Introduction

Wireless communications are an essential part of the modern information infrastructure. The last decade has been marked by the exponential spread of handsets, such as smartphones, tablets, as well as new network-dependent devices. The challenging requirements, in terms of high data-rate communication links, have driven the successive generations of standards with higher throughput, mobility-support and increased Quality-of-Service (QoS) and Quality-of-Experience (QoE). Nonetheless, all further progress must be done in a smooth and efficient manner without entailing in increased Operational Expenditure (OPEX)/Capital Expenditure (CAPEX) costs. Increasingly, this implies that the radio resources must be efficiently exploited, at the same time that higher data-rate wireless access technologies must be developed. To meet the data-rate requirements in an efficient way, the first step involved the augment of the available bandwidths in the 3G systems [1]. Then, in an attempt to achieve scalable wider bandwidths, without spectrum allocation constraints, the concept of Carrier-Aggregation (CA) was introduced in 4G systems, such as Long-Term Evolution (LTE)-Advanced [1]. By standardizing the contiguous and the non-contiguous CA capabilities, the combination of multiple frequency bands to conduct high-speed data transmission was enabled. Due to the commercial success of LTE-Advanced features, it is expected that they will continue to be evolved, as a part of 5G technologies [2].

To accomplish the Radio Access Network (RAN) expectations in a compact and efficient way, there is a strong need for the development of flexible, agile and reconfigurable radio transceivers, with a native support for multiple bands and multiple standards [3], [4]. The integration of these features seems to be of paramount importance to provide an efficient approach to the establishment of multiple, concurrent and frequency-agile data links between all the RAN parties [5].

The concept of All-Digital Transmitter (ADT) has been targeted as a promising path towards the development of the next generation of Radio-Frequency (RF) transceivers. The promising potential to design compact and versatile wireless communication transceivers has attracted much and renewed attention. They propose a fully digital datapath from Baseband (BB) up to the RF stage. This enables the design of low-complex and flexible transmitters. The block diagram of the most common ADTs found in the State-of-the-Art (SoA) (herein referred to as BB-stage ADT) is depicted in Fig. 1a. The underlying idea is the quantization of an m-bit

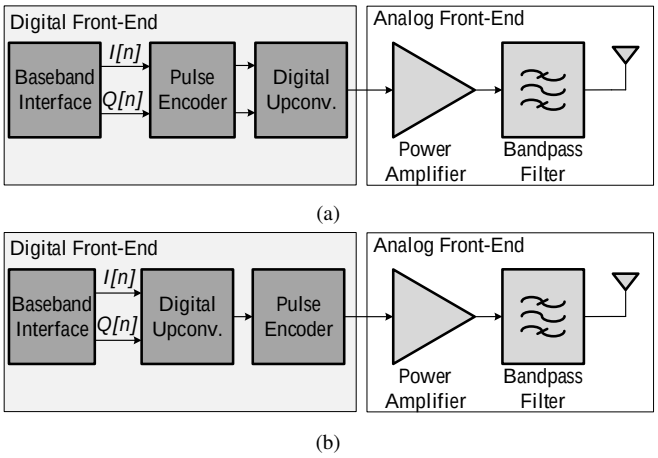

Fig. 1. Illustration of the general block diagram of a BB-stage ADT [in (a)] and an RF-stage ADT [in (b)].

digital signal into a 2-level representation, resulting in signals with constant envelope. After a digital upconversion to the desired carrier frequency, the pulsed representation can be amplified by highly-efficient and non-linear amplifiers, such as the Switched-Mode Power Amplifiers (SMPAs). After the amplification, a bandpass filter is required to reconstruct the signal before being radiated by the antenna. The fully digital behavior inherently leads to agile, flexible, reconfigurable, multi-standard, and quite important for this work, multi-band RF front-ends with minimal external front-end.

Nevertheless, despite the apparent ideal and native support for the multi-band capability, design challenges associated with the non-contiguous CA transmission have hampered the development of multi-band solutions. Within the scope of this research line, the aim of this work is the proposal of a real-time architecture that enables a wideband agility in the placement of multiple bands, at the same time that can be embedded and synthesized within a Field-Programmable Gate Array (FPGA). To meet the specifications, highly parallelized architectures, which allow high equivalent sampling rates, should be explored. In these architectures, high sampling rates can be achieved while maintaining relative lower individual sampling rates ($\leq$ 100 MHz).

The remainder of this paper is organized as follows. In Section II, the state of the technology is outlined. In Section III, the main contributions of this paper are summarized. In Section IV, a parallel concurrent triple-band transmitter architecture is proposed. Section V details the experimental results, and the conclusions are drawn in Section VI.

II. State-of-the-art

As introduced before, the reported literature on non-contiguous CA ADTs is quite limited. In general, multi-band transmission can only be achieved with integer multiples of the modulators sampling frequencies [6], or with reduced sampling rate topologies [7], [8]. Others, employ bulky and inefficient power combiners to join different bands before transmission [4], [7]. All these difficulties in designing multi-band transmission arise from the placement of the Digital Up-Conversion (DUC) after the pulse encoding (refer to Fig. 1a). Following this approach, as the encoded signals have a considerable amount of out-of-band noise distributed over the entire spectrum, the upconversion to the different bands typically leads to a degraded system performance. This issue was already introduced in [9], where a pre-compensation mechanism was proposed to minimize the amount of out-of-band noise that is folded back to the bands of interest. However, the application of this mechanism is quite limited. In fact, it can just be applied in architectures where the out-of-band noise (that falls in the desired bands) is correlated with the input signal.

In addition to that, as far as the FPGA-based architectures are concerned, the limited sampling rate from the programmable logic subsystems (typically less than 200 MHz) bounds the 1st Nyquist Zones (NZ). This considerably limits the maximum distance between different bands to twice this value [assuming complex Single-Side Band (SSB) upconversions schemes]. Thus, the one reported to achieve higher spans between bands is based on the utilization of replicas from different NZs [6]. However, the inherent decrease in terms of Signal-to-Noise Ratio (SNR), associated with the need of maintaining an integer multiplicity in all the involved sampling rates/frequencies leads to a reduced performance.

The latter paragraph is clear in the definition of the major bottleneck to the design of non-contiguous CA ADTs: the DUC is positioned after the Pulse Encoder. As previously stated, two disadvantages arose: the encoded signal is not band-limited, which may jeopardize the signal integrity of each band, and the NZ's sampling rate is too low, limiting the agility. Thus, to ensure a wideband agility, novel techniques should be followed to ensure the application of the pulse encoding after the DUC (the concept of RF-stage ADT depicted in Fig. 1b). Even though the simplicity of this concept, the limited sampling rate from the FPGA's programmable logic subsystems has precluded the implementation of this concept. Up to now, the only design methodology that enables the synthesis of such architecture into an FPGA was recently proposed in [10]. The use of highly parallelized structures to enable high equivalent sampling rates while maintaining lower individual sampling rates is reported. By doing this, it is possible to synthesize multi-rate equivalents from the DUC and the Pulse Encoder, that, ultimately, leads to the placement of the DUC before the Pulse Encoder. However, the proposed architecture has an intensive utilization of the primitive resources, as demonstrated in [10]. Thus, the replication of fully digital RF chains to enable the multi-band capability is only possible with novel design methodologies and optimization techniques.

III. Main Contributions

To the best of our knowledge, the work presented here is the first where triple-band all-digital RF-stage transmitters are completely synthesized and embedded into an FPGA. In particular, the contributions of this paper can be summarized as follows:

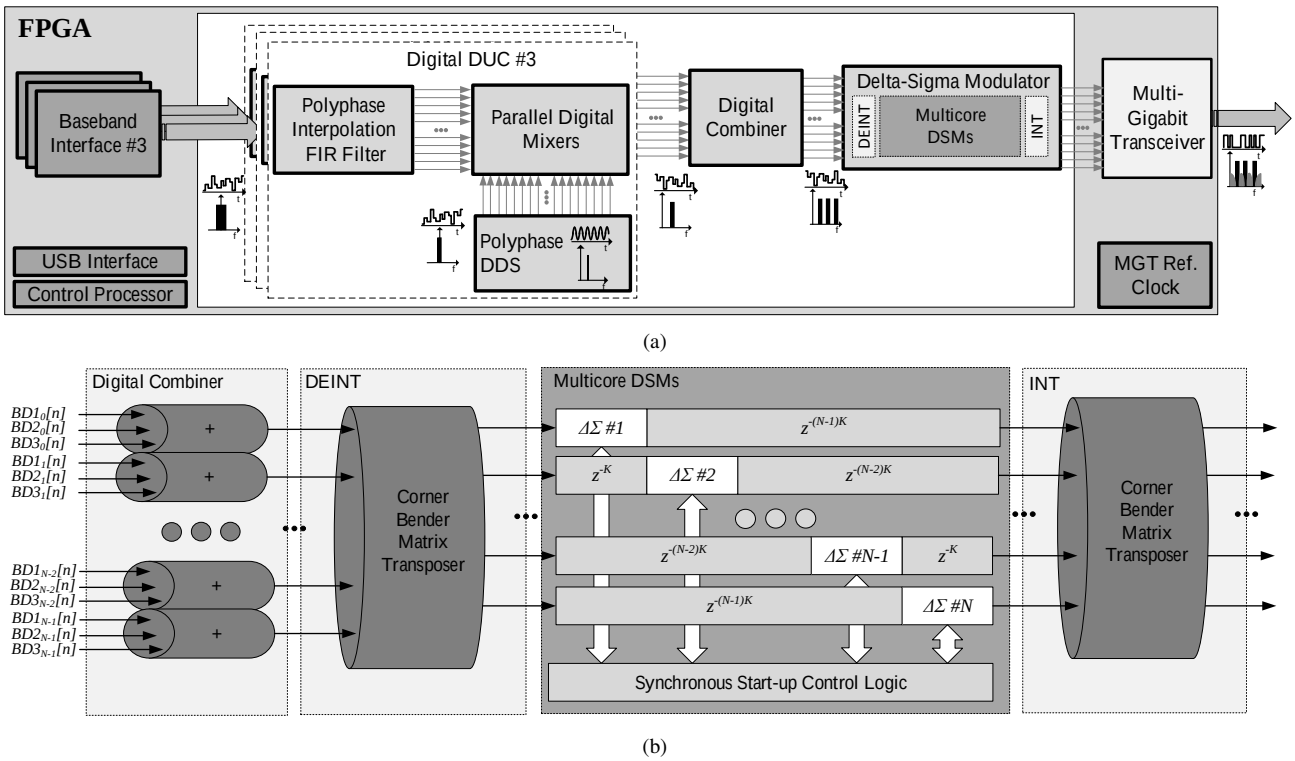

Fig. 2. (a) General block diagram of the implemented All-Digital RF transmitter, embedded into an FPGA; (b) Detailed illustration of the Digital Combiner and the Delta-Sigma Modulation ($\Delta\Sigma$M) with N parallel stages, presented in (a).

- Demonstration of a methodology to generate a Delta-Sigma ($\Delta\Sigma$) architecture with M independent and controllable Noise-Transfer Function (NTF)'s notches;
- Integration of the aforementioned $\Delta\Sigma$M in a fully parallel architecture that enables the transmission of three different RF bands. This is the first architecture embedded into an FPGA, with a maximum span of approximately 2.5 GHz;
- Proposal and integration of several optimization techniques to relax the resources usage of this architecture. First, the propagation of state registers (proposed in [11]) will be introduced as a mean to relax the resources usage, by reducing the amount of samples that must be temporarily stored (in the Deinterleaving/Interleaving Modules). Second, Corner-Bender Matrix Transposers [12] will be proposed as promising candidates to the Deinterleaving and Interleaving Modules.

It will be shown that the single-band all-digital RF-stage architecture (proposed in [10]) can be extended to enable the synthesis of multi-band RF transmitters. By taking advantage of the direct synthesis of RF waveforms in the digital domain before the Pulse Encoder, an unprecedented frequency agility is achieved. This frequency agility allows us to surpass the SoA by presenting the first concurrent multi-band all-digital RF-stage transmitter with a maximum span of almost 2.5 GHz between bands.

IV. Parallel Concurrent 3-Band Transmitter Architecture

As previously introduced, to ensure an agile multi-band transmission, the DUC stage must be applied before the Pulse Encoder. Otherwise, the maximum span will always be limited to the 1st NZ.

A. Digital Up-conversion Stage and Bands Combination

To enable the transmission of three different bands, the DUC stage must be replicated three times, as depicted in Fig. 2a. Each DUC is comprised by a polyphase interpolation Finite Impulse Response (FIR) filter, a polyphase In-phase/Quadrature (I/Q) Digital Direct Synthesis (DDS), working as a digital local oscillator, and parallel mixers. The polyphase interpolation FIR filter increases the sampling rate of the BB signal from Fs_{BB} to Fs_{RF}, dividing the samples in N different phases.

Then, N digital mixers perform the element-wise multiplication and subtraction between the interpolated samples, and the sine and cosine waveforms from the polyphase DDS. The polyphase DDS, firstly introduced in [10], combines N conventional and single-rate DDS modules. As reported in [10], the minimum frequency resolution (Δf) from this architecture is computed as follows:

$$\Delta f = \frac{Fs_{BB}N}{2^L} = \frac{Fs_{RF}}{2^L} \quad (1)$$

where L is the number of bits from each phase accumulator. The equation demonstrates that, in this architecture, the final bitrate Fs_{RF} defines the modulator's 1st NZ (from 0 to

$Fs_{RF}/2$). This means that the carrier frequency from each band can be located in any frequency bin from the frequency grid given by the DDS' frequency resolution within this NZ. Subsequently, the three interpolated and upconverted bands are combined to generate an equivalent representation with N different phases that contains the three different bands. At the same time, the resultant signal must be scaled down to the suitable Pulse Encoder's dynamic range.

B. Pulse Encoder Main Architecture

The Pulse Encoder must be designed to reduce the number of output levels, while ensuring minimal distortion in the three different bands. Moreover, the three different bands must be independently controllable and tunable, which typically implies the use of feedback loops to implement noise shaping. To accomplish these requirements, $\Delta\Sigma$ techniques were selected due to their inherent noise-shaping property that minimizes the amount of in-band distortion.

1) $\Delta\Sigma$M with Propagation of State-Registers: As previously introduced, the limited sampling rate of BB-stage ADTs presents the major bottleneck to the design of single-bit multi-band architectures. This arises from the limited BB sampling rate that inherently implies a limited 1st NZ. Thus, to ensure a wide placement of all the different bands, the Pulse Encoder's sampling rate must be increased. One way to accomplish this is based on the parallelization of $\Delta\Sigma$Ms. This was proposed in [13], and the first implementation of this architecture within an RF-stage ADT was reported in [10]. This architecture achieves high sampling rates by feeding *N* independent slices (of size *K*) from the same input signal to *N* different $\Delta\Sigma$Ms. To implement such architecture, in addition to the parallelization of N $\Delta\Sigma$Ms, two new modules were introduced: the Deinterleaving and the Interleaving module. These are mainly based on First-In First-Outs (FIFOs) and are required to accomodate and re-arrange the input/output data. The aim is to ensure that the feedback loop from each $\Delta\Sigma$Ms is processing contiguous samples of the input signal.

However, it is demonstrated in [11] that the impulsive noise caused by the discontinuities between different slices (with a period of K samples) degrade the system's performance. The most natural way to ensure a high-level of signal integrity is to increase the number of contiguous samples (K), reducing the number of glitches per second that occurs on the block transitions. Nonetheless, this leads to a considerable amount of memory-primitive resources (mainly FIFOs). A different approach is based on the propagation of the state registers between adjacent $\Delta\Sigma$Ms and it was proposed in [11]. By adopting this technique, the periodicity of the impulsive noise can be reduced by a factor of N. Thus, for a given performance, the number of contiguous samples can be lowered (by the same factor) leading to savings in the memory-primitive resources, as compared with [13]. In spite of these savings, the allocation of block Random-Access Memory (RAM) for FIFOs is not always directly proportional to K. In particular, when the number of phases N is increased, a significant amount of resources tend to be allocated regardless of the required depth, and even for low values of K. As an example, in Xilinx programmable logic systems, if the concatenation of bits is higher than 72, RAMB36E1 modules are directly chosen and allocated. In the end, entire slots of 36 kb can be allocated for only storing a few dozens of bits, leading to extremely inefficient resource usage due to the low-occupancy rate.

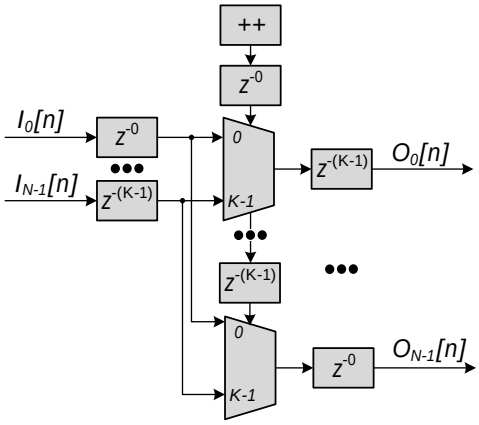

Fig. 3. Illustration of the block diagram of a Corner-Bender Matrix Transposer. The designed Interleaving and Deinterleaving modules are based on this transposer.

This inefficiency is quite exacerbated when the amount of digital subsystems is increased, which is a mandatory step in this work, in order to enable the synthesis of multi-band RF-stage transmitters. Thus, new approaches should be developed to obviate the use of FIFOs. We propose the use of a "Corner-Bender Matrix Transposer" [12] to maintain the desired functionality with just registers and multiplexers. The only requirement is the number of contiguous samples (K) to be equal to the number of parallel phases (N). While this requirement can be a limitation to the truly parallel $\Delta\Sigma$M architecture, due to the weak signal integrity (in [13]), it will be shown that, if the propagation of state registers between $\Delta\Sigma$ modulators [11] is performed, reasonable performance can be achieved. The Corner-Bender Matrix Transposer is depicted in Fig. 3. This design does not use any FIFOs, it is fully synchronous, does not require any control signal and it only uses fixed size shift register delays. The latency is the minimal possible and equal to the number of contiguous samples (K). Moreover, the same module can be used in the Deinterleaving and Interleaving subsystems. In short, it will be seen that the inclusion of this module enabled a drastic reduction on Block Random-Access Memory (BRAM) primitive resource usage.

The detailed illustration of the Pulse Encoder is depicted in Fig. 2b. One can clearly visualize the utilization of the Corner Bender Matrix Transposers as De-interleaving and Interleaving Modules (referred to as "DEINT/INT" in the illustration). In addition to this, it is also depicted the propagation of state registers through the displacement of the $\Delta\Sigma$s modulators, together with the "Synchronous Start-up Control Logic" module [11].

2) $\Delta\Sigma$M Design: A $\Delta\Sigma$ modulator must be designed and replicated *N* times, according to the architecture introduced in the last subsection. The choice of it, must be done according to two different requirements. First, the architecture must present

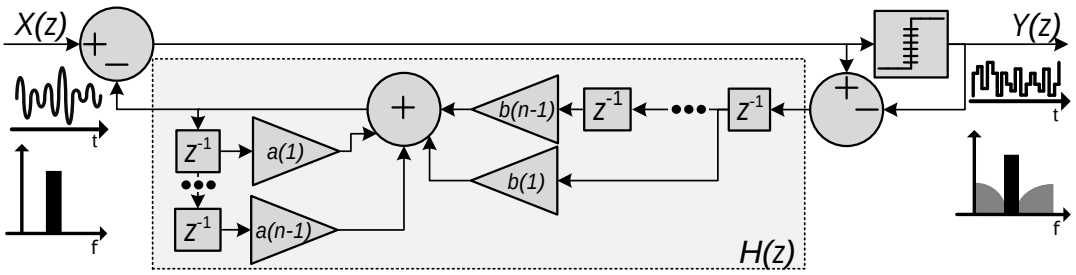

Fig. 4. Representation in z-domain of a generic Error-Feedback $\Delta\Sigma$ modulator with an Infinite Impulse Response (IIR) feedback loop. The complex poles reduce the NTF's gain, ensuring the stability of the system.

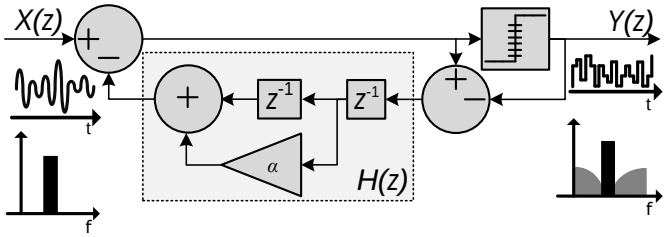

Fig. 5. Z-domain representation of the tunable 2nd order bandpass $\Delta\Sigma$ modulator.

an NTF with three well-defined notches, to ensure the integrity of the three different bands. Second, the notches must also be tunable, and independently controllable, to provide the desired real-time agility to the overall system. At last, the modulator's critical path must be as short as possible, reason for why the architectures such as Cascade-of-Resonators, FeedBack/FeedForward (CRFB/F) or Cascaded-of-Integrators, FeedBack/FeedForward (CIFB/F) can not be chosen.

Thus, the Error-Feedback $\Delta\Sigma$ architecture (depicted in Fig. 5) was selected as a starting point for this work. By modeling the quantization noise by a random noise signal ($E_q(z)$), the following transfer function can be derived:

$$Y(z) = STF(z)X(z) - NTF(z)Eq(z) \tag{2}$$

where $STF(z) = 1$, $NTF(z) = (1 + H(z))$ and $H(z) = \alpha z^{-1} + z^{-2}$. The modulator's behavior depends on the variable α, defined as $\alpha = -2\cos(2\pi F_{c1}/Fs)$, where F_{c1} is the notch center frequency and Fs is the modulator's sampling rate. In particular, it has two complex zeros that allow the adjusment of the notch carrier as desired.

An intuitive approach to achieve a triple band modulator could pass through the inclusion of 2 pairs of other complex zeros, defined by β and γ:

$$NTF(z) = \left(1 + \alpha z^{-1} + z^{-2}\right).\left(1 + \beta z^{-1} + z^{-2}\right). \\ .\left(1 + \gamma z^{-1} + z^{-2}\right) \tag{3}$$

where $\beta = -2\cos(2\pi F_{c2}/Fs)$, $\gamma = -2\cos(2\pi F_{c3}/Fs)$ with F_{c2} and F_{c3} being the notches center frequencies.

However, for the used wireless modulated signals, this architecture may lead to stability issues, specifically depending on the notches placement. Thus, to control the NTF's gain, complex poles must also be included, leading to the generic Error-Feebdack $\Delta\Sigma$ modulator with an IIR feedback loop that is depicted in Fig. 4. In the present case, 6 complex poles were integrated in the architecture. Each pair of poles closely follows each pair of zeros, to ensure the stability of the system, according to [14]. This leads to:

$$NTF(z) = \frac{1 + \alpha z^{-1} + z^{-2}}{1 + r\alpha z^{-1} + r^2 z^{-2}} . \frac{1 + \beta z^{-1} + z^{-2}}{1 + r\beta z^{-1} + r^2 z^{-2}} . \\ . \frac{1 + \gamma z^{-1} + z^{-2}}{1 + r\gamma z^{-1} + r^2 z^{-2}} \tag{4}$$

where r ranges from 0 to 1, and controls the closeness between poles and zeros. This equation can be simplified to:

$$NTF(z) = \\ = \frac{1 + A_0 z^{-1} + B_0 z^{-2} + C_0 z^{-3} + D_0 z^{-4} + E_0 z^{-5} + z^{-6}}{1 + F_0 z^{-1} + G_0 z^{-2} + H_0 z^{-3} + I_0 z^{-4} + J_0 z^{-5} + K_0 z^{-6}} \tag{5}$$

where $A_0 = (\alpha + \beta + \gamma)$, $B_0 = (3 + \alpha\beta + \gamma(\alpha + \beta))$, $C_0 = (2(\alpha + \beta) + \gamma(2 + \alpha\beta))$, $D_0 = (3 + \alpha\beta + \gamma(\alpha + \beta))$, $E_0 = (\alpha + \beta + \gamma)$, $F_0 = r(\alpha + \beta + \gamma)$, $G_0 = r^2(3 + \alpha\beta + \gamma(\alpha + \beta)$, $H_0 = r^3(2(\alpha + \beta) + \gamma(2 + \alpha\beta)$, $I_0 = r^4(3 + \alpha\beta + \gamma(\alpha + \beta)$, $J_0 = r^5(\alpha + \beta + \gamma)$ and $K_0 = r^6$.

In turn, the feedack loop transfer function ($H(z)$) can also be computed:

$$H(z) = \\ = \frac{A_1 z^{-1} + B_1 z^{-2} + C_1 z^{-3} + D_1 z^{-4} + E_1 z^{-5} + F_1 z^{-6}}{1 + F_0 z^{-1} + G_0 z^{-2} + H_0 z^{-3} + I_0 z^{-4} + J_0 z^{-5} + K_0 z^{-6}} \tag{6}$$

where $A_1 = (\alpha + \beta + \gamma)(1 - r)$, $B_1 = (3 + \alpha\beta + \gamma(\alpha + \beta))(1 - r^2)$, $C_1 = (2(\alpha + \beta) + \gamma(2 + \alpha\beta))(1 - r^3)$, $D_1 = (3 + \alpha\beta + \gamma(\alpha + \beta))(1 - r^4)$, $E_1 = (\alpha + \beta + \gamma)(1 - r^5)$ and $F_1 = (1 - r^6)$.

The impact of placing poles in $H(z)$ in terms of magnitude of the NTF is depicted in Fig. 6. The magnitude is reduced, mitigating the potential instability. However, as a consequence, the notches' processing bandwidth becomes lower.

C. Extension to Multi-Level Output

As will be seen in Section V, the single-bit architecture in Fig. 2 was experimentally validated with successful results in terms of agility in the bands' placement. However, to enhance the system performance (assessed in terms of Adjacent-Channel Power Ratio (ACPR), Error-Vector Magnitude (EVM) and Modulation Error Ratio (MER)), a final stage that performs an extension to a multi-level output was included. The synthesis of this multi-level output is based on the combination

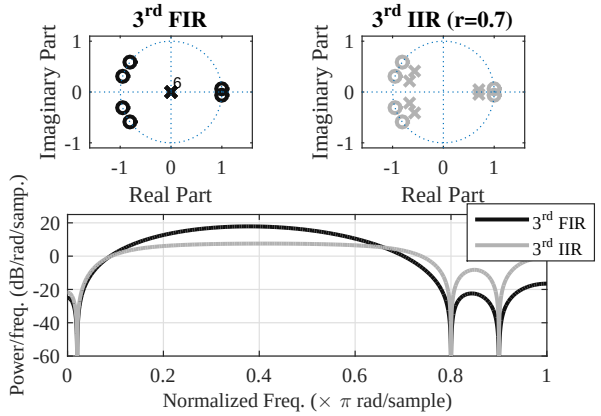

Fig. 6. NTF's frequency response and zero-poles placement according to the different feedback-loop transfer functions.

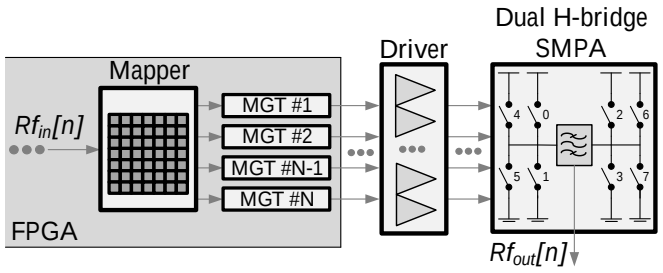

Fig. 7. Detailed illustration of the proposed amplification scheme based on an extended H-bridge SMPA

of pulsed trains. The final architecture is depicted in Fig. 8. Three major differences can be pointed out: the single-bit quantizer from each $\Delta\Sigma$M was replaced by a 7-level quantizer; 7 different Multi-Gigabit Transceivers (MGTs) were activated instead of just 1; and a Look-Up Table Mapper was included before the MGTs. This Look-Up Table Mapper is the core of this last stage and converts a multi-level input signal into a combination of 7 different pulsed train sequences. The mapper must be designed according to the used analog combination network.

The envisioned combination network to be applied in this architecture was firstly proposed in [15], and an extension to 5-level was later reported in [16]. This increase in the number of levels is possible due to the use of an Asymmetric Extended H-bridge Combining Network, whose conceptual diagram is depicted in Fig. 7. In particular, the switches from 4 up to 7 should have double size transistors when compared to the remaining ones. In the case of this combining network, the mapper is depicted in Table I. In particular, one can realize that this mapper can generate a 3-level output (dark gray background), a 5-level output (dark gray and light gray background), or a 7-level output (by using all the table elements).

Due to the lack of a proper combining network based on this proposal, another option had to be chosen for the sake of validating the proof-of-concept. Thus, a conventional RF Power Combiner was utilized to perform the combination of the different serializers' outputs, given the absence of extended H-bridge SMPA at the experiment stage. In this case, the

TABLE I
PROPOSED MAPPER FOR THE AMPLIFICATION SCHEME DEPICTED IN FIG. 7

RF_{in}	MGT_0	MGT_1	MGT_2	MGT_3	MGT_4	MGT_5	MGT_6	MGT_7
3	1	0	0	1	1	0	0	1
2	0	0	0	0	1	0	0	1
1	1	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0
-1	0	1	1	0	0	0	0	0
-2	0	0	0	0	0	1	1	0
-3	0	1	1	0	0	1	1	0

TABLE II
IMPLEMENTED MAPPER FOR THE USE OF ASSESSMENT OF THE MULTI-LEVEL OUTPUT WITH A POWER-COMBINER

RF_{in}	MGT_0	MGT_1	MGT_2	MGT_3	MGT_4	MGT_5	MGT_6	MGT_7
3	1	1	1	1	1	1	1	1
2	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	0	0
0	1	1	1	1	1	0	0	0
-1	1	1	1	1	0	0	0	0
-2	1	1	1	0	0	0	0	0
-3	1	1	0	0	0	0	0	0

mapper had to be updated to Table II. This new mapper can be simply seen as the linear combination of the pulse trains in order to achieve a higher number of output levels. One can also realize from Table II that the column related to the MGT_0 is constant. This means that one of the serializers could be removed. However, we decided to keep it to maintain the coherency with our ideal combining network based on the H-bridge.

V. EXPERIMENTAL RESULTS

This section presents and discusses the experimental setup and the measured results. In addition to that, this work is compared to other architectures found in the SoA.

To validate the proposed multi-band architecture, the two different ADTs (depicted in Figs. 2 and 8) were implemented in a Virtex 7 XC7VX485T FPGA using the Xilinx FPGA VC707 Evaluation Kit. Some details related to the fixed-point precision of all the major modules are reported in Table III.

The critical path in the single-bit project imposed a maximum Fs_{BB} of 78.125 MHz, and consequently, the bitrate of 5 Gbps was chosen. For the multi-level case, the implementation of a multi-bit quantizer caused a reduction of the maximum BB sampling rate down to 62.5 MHz, leading to the serializer's bitrate of 4 Gbps. The frequency resolutions can be computed by (1). In particular, the different bitrates together with the 10-bit resolution of the DDS' phase accumulator lead to 4.8828 MHz and 3.906 MHz of frequency resolution, for the single-bit and 7-level case, respectively.

The experimental setups are depicted in Fig. 9 and Fig. 13, for the single- and multi-bit projects, respectively. In the first one, the MGT was directly connected to a Vector Signal Analyzer (VSA) Keysight EXA N9010A. In the multi-bit project, lane-to-lane deskew techniques were implemented in the digital hardware, as well as extra phase alignment cables were attached to some MGTs to ensure the lane-to-lane synchronization. Moreover, the amplitude swing of

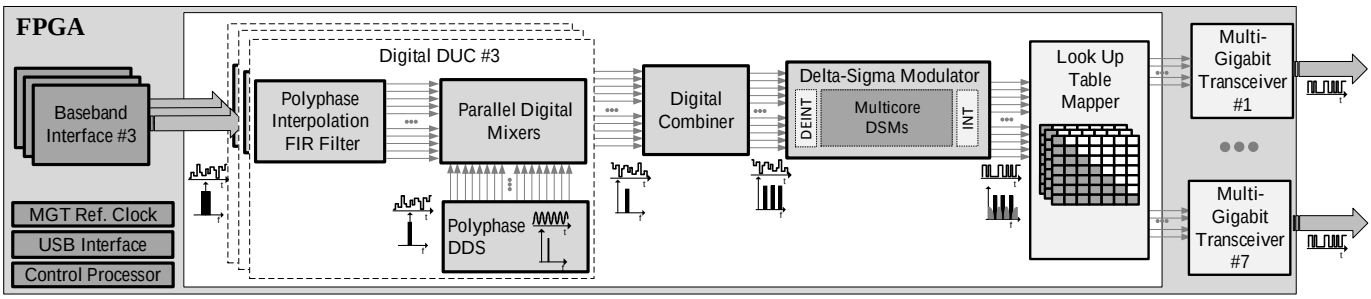

Fig. 8. General block diagram of the implemented All-Digital RF transmitter, embedded into an FPGA with an extension to a multi-level output. The Look-Up Table (LUT) performs the mapping between the different amplitude levels and the pulsed trains that drive multiple MGTs.

TABLE III
FIXED-POINT PRECISION AT THE OUTPUT OF THE DIFFERENT STAGES DEPICTED IN FIGS. 2 AND 8[1]

	Single-bit		Multi-bit	
	No. Bits	Bin. Point	No. Bits	Bin. Point
BB Interf. Ouput	11	9	11	9
Interp. Filter Ouput	11	9	11	9
DDS Accum. Ouput	10	0	10	0
DDS ROM Output	11	9	11	9
Bands Comb. Output	11	9	11	9
DUC Output	12	9	12	9
$\Delta\Sigma$ Output	1	0	3	0

[1]In the table, "n/a" stands for "not-applicable", and ROM for Read-Only Memory.

each MGT was slightly changed to ensure the same output power. Afterwards, the 7 MGTs were combined into a Power Combiner ZN8PD1-63W+ from Mini-Circuits. The combined output was connected to the same VSA. The VSA was configured to perform ACPR measurements as well to record the I/Q data to be further analyzed in the VSA LabView Software running in the computer. To enable the sweep of different carrier frequencies, modulations, bandwidths, and to record such Figures of Merit (FoM) as spectrum, MER and EVM, an automated testbed was developed. This testbed has the host computer controlling/managing the FPGA-based ADT through a USB connection and connected to the VSA through an Ethernet connection.

One note related to the sweep of carrier frequencies must be highlighted. As our system is generating three different bands, it is important to define the relative placement of the remaining carriers while a given carrier frequency is being swept. Here, several different scenarios could be explored. For instance, the three different carriers could be placed with a minimal separation between them (such as in Contiguous CA). While the band in the middle would present the best Adjacent-Channel Power Ratio Upper (ACPR-U) and Adjacent-Channel Power Ratio Lower (ACPR-L), the one at the left would present a worst ACPR-L and a better ACPR-U, and so on. Thus, to be fair in the report of the results, it was decided to place the carrier to be swept alone, and the remaining ones together. The spectra depicted in Figs. 12 and 16 can provide a better insight about the followed procedure. In this case, the band at the left was swept and measured, while the other two were maintained together in a constant distance from the

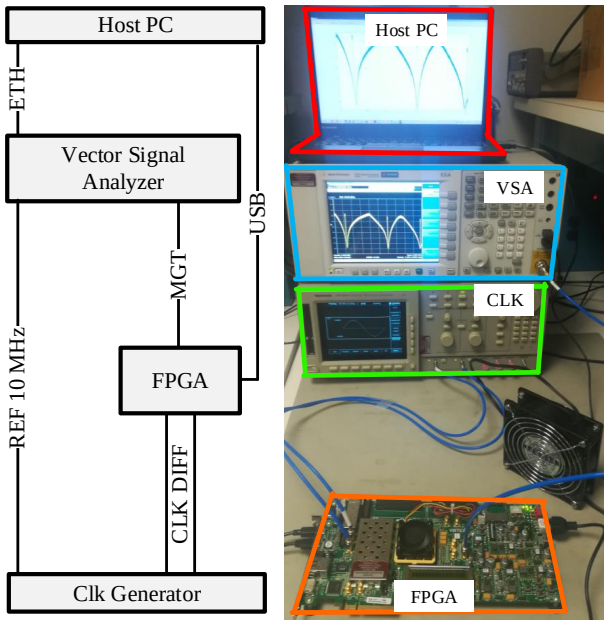

Fig. 9. Block diagram and photo of the experimental setup according to the single-bit architecture in Fig. 2.

interest carrier frequency. In this case, the remaining bands started in the right side of the center frequency of the NZ ($Fs_{RF}/4$) and ended in the left side of the center frequency. In our point of view, this approach is quite fair, by presenting the worst results that can be obtained with this implemented architecture, for the given scenario.

A. Single-bit 3-Band RF Transmission

This section details the experimental results for the Single-bit project, whose experimental setup is depicted in Fig. 9.

Fig. 10 shows the measured ACPR results (lower and upper) in the range of 100 MHz up to 2.5 GHz, with a step of 48.828 MHz for three different bandwidths per band: 4.688 MHz, 9.375 MHz and 18.75 MHz. It can be seen that all the measurements maintain the same coherency: the increase of the bandwidth leads to higher quantization noise around the carrier frequencies, which consequently, increases the ACPR values. The signals with higher bandwidth present the worst results in terms of ACPR: between -20 and -30 dBc.

MER and EVM obtained pairs are reported in Fig. 11. Again, the same intuitive conclusions can be extracted. Narrow

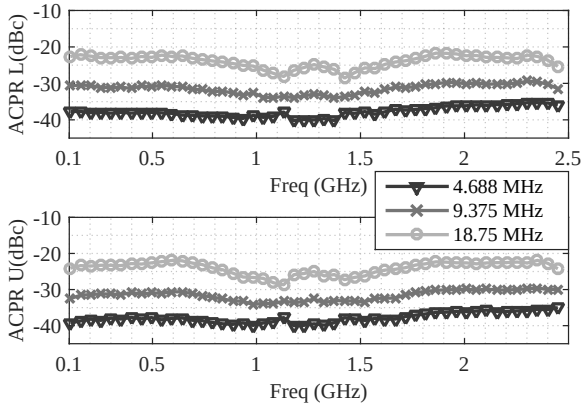

Fig. 10. Measured ACPR-L and ACPR-U results of a sweep in the carrier frequency with a 16-QAM modulated signal with 4.688, 9.375 and 18.75 MHz of bandwidth.

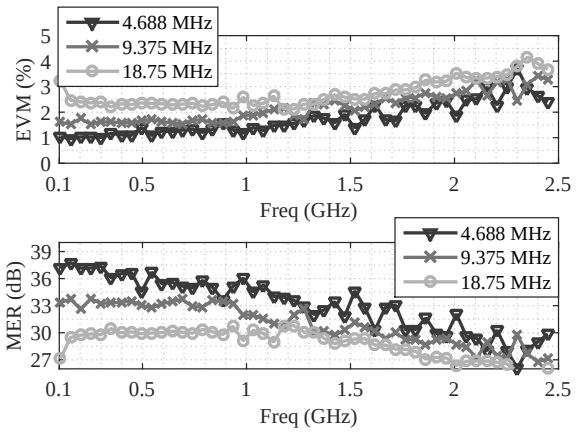

Fig. 11. Measured EVM and MER results of a sweep in the carrier frequency with a 16-QAM modulated signal with 4.688, 9.375 and 18.75 MHz of bandwidth.

bandwidths provide better FoMs. In particular, the maximum obtained MERs were 38, 35 and 31.5 dB, for the aforementioned bandwidths.

The spectrum in a span of 2.5 GHz, for carrier frequencies of 600.59 MHz, 2.002 and 2.4023 GHz, is shown in Fig. 12.

Finally, the occupied resources in the FPGA for the proposed architecture are presented in Table IV. A high percentage of DSP slices is used in the parallel $\Delta\Sigma$M, as well as in the polyphase interpolation FIR filters. These filters were designed with a four-tap transposed direct-form architecture per phase. In this project, the BRAM is just being used to accommodate the multiple DDS's Read-Only Memory (ROM). Nonetheless, depending on the requirements, there is enough margin to implement a even more efficient memory usage through the exploration of the symmetry of the DDS' sinusoidal waveforms. At last, we consider that the inclusion of the Corner-Bender Matrix Transposer was quite successful, because no BRAM is being used in the Deinterleaving/Interleaving modules.

B. 7-Level 3-Band RF Transmission

This subsection details the experimental results for the concurrent 7-level 3-Band RF Transmission, whose experimental

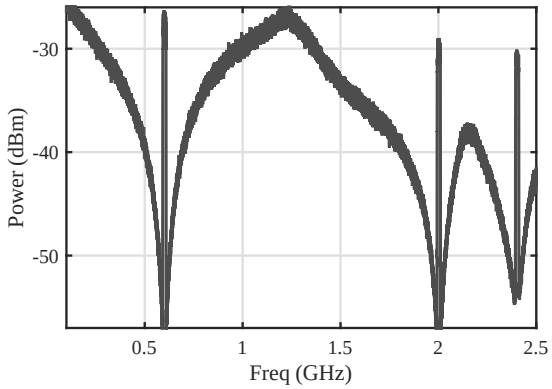

Fig. 12. Obtained spectrum with a full span of 2.5 GHz for carrier frequencies of 600.59 MHz, 2.002 and 2.4023 GHz, with a bandwidth of 18.75 MHz.

TABLE IV
OCCUPIED RESOURCES FOR THE PROPOSED SINGLE-BIT RF TRANSMITTER DESIGN

Logic Resources	Used	Total	%
Flip Flops	164944	607200	27.16
LUTs	113123	303600	37.26
Memory LUT	60045	130800	45.91
BRAM	192	1030	18.64
DSP48	1876	2800	67.00
GTXs	1	27	3.7

setup is depicted in Fig. 13.

Fig. 14 shows the measured ACPR results (lower and upper) in the range of 100 MHz up to 2.0 GHz, with a step of 39.062 MHz for five different bandwidths per band: 3.75 MHz, 7.5 MHz, 15 MHz, 18.75 MHz and 37.5 MHz. It can be seen that all the measurements maintain the same coherency: the increase of the bandwidth leads to higher quantization noise around the carrier frequencies, with the inherently increase in the ACPR values. The signals with higher bandwidth present the worst results in terms of ACPR: between -20 and -30 dBc. By comparing this figure with the single-bit one (Fig. 10), it is understandable the impact of using a multi-bit quantizer: the same results were achieved with twice the signal bandwidth.

MER and EVM obtained pairs are demonstrated in Fig. 15. Due to the limited available I/Q bandwidth from the VSA (25 MHz), it was not possible to get some measurements for the 37.5 MHz case. Again, the same intuitive conclusions can be extracted. Narrow bandwidths provide better FoMs. In particular, the maximum obtained MERs were 38, 37, 36 and 34 dB, for the aforementioned bandwidths.

The spectrum in a span of 2.0 GHz, for carrier frequencies of 500 MHz, 1.6016 and 1.9219 GHz is shown in Fig. 16.

As a final note, it is important to highlight that the gains in terms of in-band performance were not the ones expected. As ideally almost 3 bits are available in the output, the theoretical in-band performance gains should be approximately 12 dB. Thus, simulations were carried out to understand this drop of performance, and it was possible to conclude that it was caused by the non-ideal timing alignment and amplitude matching between multiple lanes. However, on the other hand, as far as the out-of-band noise is concerned, by comparing spectra

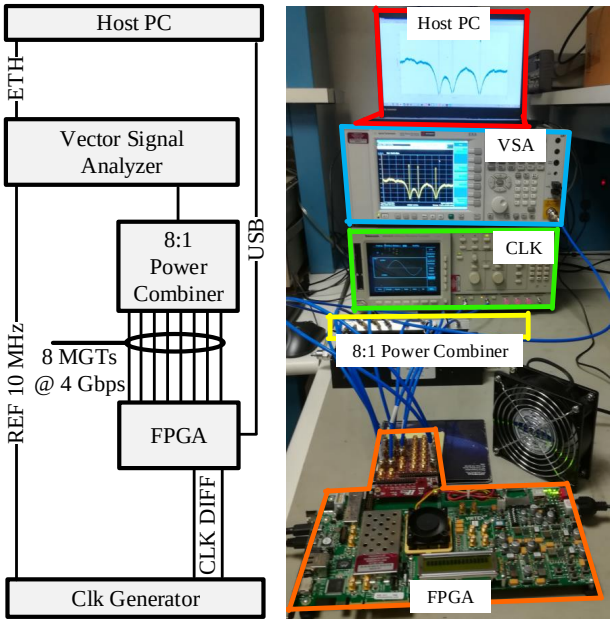

Fig. 13. Block diagram and photo of the experimental setup according to the 7-level architecture in Fig. 8.

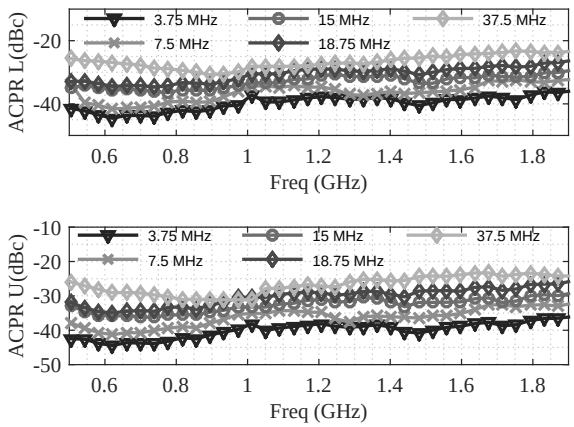

Fig. 14. Measured ACPR-L and ACPR-U results of a sweep in the carrier frequency with a 16-QAM modulated signal with 3.75, 7.5, 15, 18.75 and 37.5 MHz of bandwidth.

in the single-bit (Fig. 12) and the multi-bit output (Fig. 16), one can verify that the quantization noise power is actually reduced. In the single-bit spectra, the quantization noise power reaches a maximum value of -28 dB while in the multi-bit spectra this value is reduced to -40 dB.

Finally, the occupied resources for the 7-level case are shown in Table VI. The results are quite similar to the ones reported in the single-bit project.

C. Comparison to the SoA

Table V presents an overview of the relevant modulators presented in the literature. The table aimed to focus on the number of transmitted bands, the achieved bandwidth per band, the maximum span between bands, the serializer's sampling rate, the modulator type, the number of levels from the output signal, the number of transmitters, the dependence

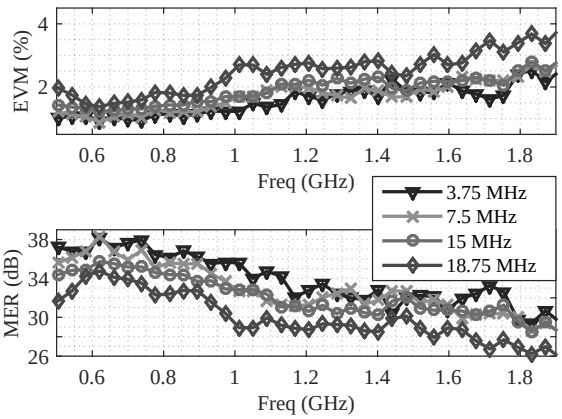

Fig. 15. Measured EVM and MER results of a sweep in the carrier frequency with a 16-QAM modulated signal with 3.75, 7.5, 15 and 18.75 MHz of bandwidth.

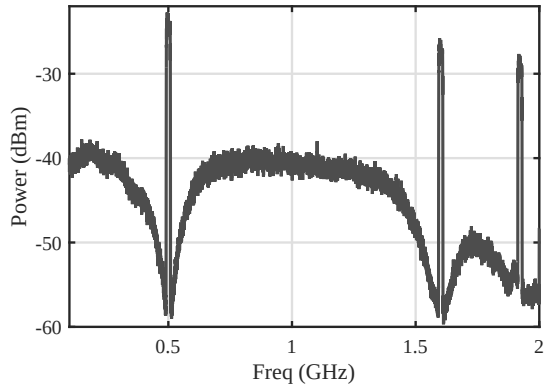

Fig. 16. Obtained spectrum with a full span of 2.5 GHz for carrier frequencies of 500 MHz, 1.6016 and 1.9219 GHz, with a bandwidth of 18.75 MHz.

of the carrier frequency with the serializer carrier frequency, the hardware implementation and, last but not least, the agility. By agility, we are referring to implementations or techniques that allow the adjustment of the carrier frequency without changing the output's sampling rate.

Clearly, the two proposed implementations surpass the SoA in several aspects. In the first place, they are the first reported architectures that enable the synthesis of three different bands with maximum spans of 2.5 and 2 GHz within an online FPGA implementation. The maximum spans from the SoA (1 and 1.8 GHz) were achieved with offline FPGA/Arbitrary Waveform Generator (AWG) implementations [8], [17].

The proposed architectures also demonstrated the highest bandwidth per band (18.75 and 37.5 MHz), leading to the highest aggregated bandwidth (56.25 and 112.5 MHz) from all the SoA. The previous maximum aggregated bandwidth (40 MHz) was reported in [18] with an offline 5-bit AWG implementation.

In addition to that, it must be pointed out that this work presents no additional Over Sampling Ratio (OSR) between the maximum span and the output sampling rate (generation is possible up to the Nyquist limit). Ultimately, this leads to the minimal output sampling rate, which is essential to minimize

TABLE V
COMPARISON OF THE PROPOSED ARCHITECTURES WITH SOME RELEVANT MODULATORS FROM THE SOA[2]

Reference	No. Bands	BW per Band (MHz)	Max. Span (GHz)	Fout (Gbps)	Mod. Type	No. Lev.	No. Tx	Fc indep. Fout	HW. Impl.	Agility
This (Impl. 1)	**3**	**18.75**	**2.5**	**5**	**3rd EF RF-BPDSM**	**2**	**1**	**Yes**	**FPGA online**	**Yes**
This (Impl. 2)	**3**	**37.5**	**2**	**4**	**3rd EF RF-BPDSM**	**7**	**7**	**Yes**	**FPGA online**	**Yes**
[8] (Impl. 1)	2	5	0.7	3.9	6th CRFB RF-BPDSM	2	1	Yes	FPGA offline	No
[8] (Impl. 2)	3	5	1	3.9	6th CRFB RF-BPDSM	2	1	Yes	FPGA offline	No
[17]	3	10	1.8	7	4th CRFB RF-BPDSM	33	2	Yes	AWG offline	No
[18]	2	20	0.60	24.5	6th CRFB RF-BPDSM	3	2	Yes	AWG offline	No
[9]	2	3.75	0.25	10	1st EF BB-BPDSM	2	1	No	FPGA online	Lim.
[6]	2	2	0.45	7.2	2nd CIFB BB-LPDSM	2	1	No	FPGA online	Lim.
[19]	3	<2	0.378	9	2nd CIFB BB-LPDSM	2	2	No	FPGA online	Lim.
[7]	2	10	0.6	6.14	8th CRFB BB-BPDSM	4	3	No	Simul.	-

[2]In the table, "n/a" and "-" stand for "not-available" and "not-applicable", respectively.

TABLE VI
OCCUPIED RESOURCES FOR THE MULTI-LEVEL RF TRANSMITTER DESIGN

Logic Resources	Used	Total	%
Flip Flops	174533	607200	28.58
LUTs	140027	303600	46.12
Memory LUT	74004	130800	56.58
BRAM	192	1030	18.64
DSP48	1876	2800	67.00
GTXs	7	27	25.9

the switching losses from the amplification stage.

Lastly, one can also recognize that the proposed architectures are the first ones from the SoA to achieve a real-time agility. This means that the three bands can be located in any bin from the frequency grid given by the DDS' frequency resolution within the 1st NZ (2.5 and 2 GHz, in the single-bit and multi-bit implementations, respectively). All the other approaches based on FPGA online implementations did not possess this capability, due to the fact that the DUC was applied after the Pulse Encoder (the concept of BB-stage ADTs). It must also be mentioned that, as proposed in [10], when a fine frequency resolution is required, a single-rate digital-Intermediate Frequency (IF) together with a single-rate high-resolution DDS can be included before the polyphase interpolation FIR filter of each band.

One final note related to the scalability of this architecture must be highlighted. The main focus of this work was the proposal of a fully agile multi-band RF-stage transmitter, suitable for contiguous/non-contiguous CA scenarios, that could be embedded into programmable logic. First, even though we have implemented a triple-band RF transmitter, the formulated design methodology is independent of the number of bands. However, each time that more bands are included, there is an additional increase in the critical path that forces the reduction of the serializer's sampling rate. In addition to this, more resources are also required. Thus, from a system designer's point-of-view, the inclusion of optimization techniques in terms of timing/area must be adopted. As an example, a different work demonstrated in [20] shows that the careful placement of the NTF zeros can leverage the implementation of optimization strategies with constant multipliers that can boost the global sampling rate. In that specific work, a sampling rate of 10 Gsps was achieved with a 3rd-order FIR feedback loop in the $\Delta\Sigma$M. The same work was also the starting point in the optimization of the Deinterleaving/Interleaving modules that culminated in the use of Corner-Bender Matrix Transposers in this work. As far as the resources usage is concerned, it must be highlighted that, the amount of logic resources that were reported in both implementations should not be taken as the minimum required values. Several different optimization techniques, in the critical subsystems, can always be done according to different requirements.

In the end, it can be concluded that the proposed parallel architecture has a large potential for the design of real-time multi-band reconfigurable digital RF transmitters. In addition to the single-bit architecture, the advantages of increasing the number of bits in the output are demonstrated, as well as a promising amplification chain based on asymmetric extended H-bridge SMPA was illustrated (Fig. 7). This type of chain enables the amplification of a multi-level signal, through the combination of several amplified pulsed trains. Thus, highly-efficient and non-linear amplification techniques are explored regardless of the Peak-to-Average Power Ratio (PAPR) of the modulated signal. Moreover, instead of putting effort in minimizing the quantization noise power in the analog domain, we demonstrated that we could actually reduce the quantization noise power that is being generated in the digital domain. In

the end, this strategy has a twofold advantage: reduces the requirements for the analog reconstruction filter at the same time that ensures higher in-band performance in the generated signal. In this viewpoint, we also demonstrate how this can be implemented in our architecture: replacing the single-bit quantizer by a multi-bit quantizer, and introducing a LUT mapper that performs the mapping from a multi-level signal to pulsed trains. We consider that our approach of using the conventional RF Power Combiner with an alternative mapper validates our point-of-view, at the same time that demonstrates the practical gains that can be achieved (higher ACPR, higher MER, lower filtering requirements), as well as the practical limitations that every designer needs to take into consideration: the synchronization and the amplitude impairments between multiple lanes. In addition to that, the real-time reconfiguration of all the architecture involves a small change in the set of variables that control the polyphase DDSs, and the polyphase $\Delta\Sigma$Ms.

VI. Conclusion

In this paper, a novel architecture for designing agile and real-time reconfigurable ADTs for contiguous or non-contiguous CA scenarios was presented. The technique was proposed and validated on an FPGA. The reported results demonstrate a superior performance in terms of agility (from 0.1 up to 2.5 GHz), maximum span between bands (up to 2.5 GHz) and aggregated bandwidth (up to 56.25 MHz). To enhance the system performance, an extension to a multi-level architecture was also proposed, enabling the transmission of 112.5 MHz of aggregated bandwidth. In addition to the superior performance, as compared to the SoA counterparts, the fully digital behavior of this architecture shows a strong potential to be synthesized in custom application specific integrated circuits. This work demonstrated the feasibility of software-defined radio techniques for agile and concurrent multi-band transmission for LTE-Advanced and beyond mobile communications.

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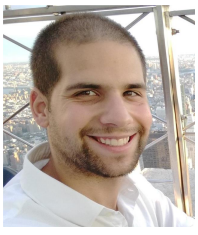

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