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Ferroelectric memory field-effect transistors using CVD monolayer MoS2 as resistive switching channel

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Abstract

Ferroelectric field-effect transistors (FeFETs) have been considered as promising electrically switchable nonvolatile data storage elements due to their fast switching speed, programmable conductance, and high dynamic range for neuromorphic applications. Meanwhile, FeFETs can be aggressively shrunk to the atomic scale for a high density device integration, ideally, without comprising the performance by introducing two-dimensional (2D) materials. So far, the demonstrated 2D material-based FeFETs mainly rely on mechanically exfoliated flakes, which are not favorable for large-scale industrial applications, and FeFETs based on organic ferroelectrics typically show a large writing voltage (e.g., >620 V), making these types of memory devices impractical to be commercially viable. Here, we demonstrate that monolayer MoS2 grown by chemical vapor deposition (CVD) can be used as a resistive switching channel to fabricate FeFETs, in which the MoS2 channel is modulated by a hybrid gate stack of HfO2/ferroelectric HfZrOx thin films. The programming processes in the 2D MoS2 FeFETs originate from the ferroelectric polarization switching, yielding two distinct write and erase states for data storage and cumulative channel conductance for artificial synapse applications. Our 2D FeFETs show a low-voltage-driven feature (<63 V) and gate-tunable ferroelectric hysteresis characteristics. The thin HfO2 layer in the hybrid gate stack likely plays crucial roles in preserving the ferroelectricity of the device and lowering the threshold of switching voltages through energy redistribution. Our findings open an avenue for the use of CVD-grown layered materials as the resistive switching mediums combined with HfO2-based ferroelectrics for future energy-efficient “brain-on-a-chip” hardware.

Applied Physics Letters

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ABSTRACT

Ferroelectric field-effect transistors (FeFETs) have been considered as promising electrically switchable nonvolatile data storage elements due to their fast switching speed, programmable conductance, and high dynamic range for neuromorphic applications. Meanwhile, FeFETs can be aggressively shrunk to the atomic scale for a high density device integration, ideally, without comprising the performance by introducing two-dimensional (2D) materials. So far, the demonstrated 2D material-based FeFETs mainly rely on mechanically exfoliated flakes, which are not favorable for large-scale industrial applications, and FeFETs based on organic ferroelectrics typically show a large writing voltage (e.g., $>\pm 20$ V), making these types of memory devices impractical to be commercially viable. Here, we demonstrate that monolayer MoS_2 grown by chemical vapor deposition (CVD) can be used as a resistive switching channel to fabricate FeFETs, in which the MoS_2 channel is modulated by a hybrid gate stack of HfO_2/ferroelectric $HfZrO_x$ thin films. The programming processes in the 2D MoS_2 FeFETs originate from the ferroelectric polarization switching, yielding two distinct write and erase states for data storage and cumulative channel conductance for artificial synapse applications. Our 2D FeFETs show a low-voltage-driven feature ($<\pm 3$ V) and gate-tunable ferroelectric hysteresis characteristics. The thin HfO_2 layer in the hybrid gate stack likely plays crucial roles in preserving the ferroelectricity of the device and lowering the threshold of switching voltages through energy redistribution. Our findings open an avenue for the use of CVD-grown layered materials as the resistive switching mediums combined with HfO_2-based ferroelectrics for future energy-efficient "brain-on-a-chip" hardware.

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The ever-increasing demand for energy-efficient and high-speed data processing and storage has triggered the research community to look for new electronic materials and device architectures.[1] For this reason, the family of two-dimensional transistor metal dichalcogenides (2D TMDs) has attracted considerable attention since the successful exfoliation of graphene in 2004.[2] Though graphene does not have a bandgap, TMD crystals, when reaching the single-layer limit, can possess sizable direct bandgaps with moderate carrier mobilities and rich physical properties for various applications, including transistors,[3] photodetectors,[4] energy harvesting devices,[5] and spintronics.[6] Combined with their ultimate thinness in vertical dimensions, devices based on 2D TMDs are highly desirable for the compact integration of computing chips, logic, and memory cells with further reduction in power consumption enabled by the strong coupling between the gate electric fields and their ultrathin bodies. Among all TMDs, molybdenum disulfide (MoS_2) is noteworthy because of its relatively high chemical stability and large bandgap (1.8–1.9 eV).[7] High-performance transistors and optoelectronics based on MoS_2 have been reported.[3,8,9] However, detailed investigations of its applications for data storage devices based on different device architectures are still lacking.

Very recently, layered 2D materials have been introduced into various types of emerging memory technology based on resistive switching through either electrical or optical excitations such as two-terminal memristors and optical memory devices.[10–14] Given the excellent properties that MoS_2 holds as the transistor channel, memory devices adopting the field-effect transistor (FET) architectures, namely, ferroelectric FETs (FeFETs), would be a promising strategy to integrate MoS_2 into high-performance data storage systems, where a high-density memory

cell array and a low operational power are highly desired. Ferroelectric-based memory devices ideally exhibit nonvolatility, fast switching, a high on/off ratio, and programmable multilevel conductance states for applications in artificial neural networks.[15–20] Until now, organic ferroelectric polymers have been widely used in promising FeFETs due to the advantages of large-scale preparation and mechanical flexibility.[9,18,19,21] Nevertheless, since organic ferroelectric materials are usually highly soluble in common organic solvents and show low thermal budgets, integrating organic ferroelectric-based devices into integrated circuits (ICs) could be challenging, considering that high-performance computing systems require complicated semiconductor manufacturing processes. Moreover, those organic FeFETs in general show high writing voltages (e.g., $\pm$35 V for the 2D $MoSe_2$ FeFET),[18] likely due to the spin-coating-process-limited thickness of the ferroelectric poly (vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] layer ($\sim$300 nm), which limits the gate control efficiency. Those aforementioned limitations make such types of FeFETs difficult to be commercially feasible. On the other hand, attempts at building high-performance FeFETs using 2D TMD channels have so far relied on mechanically exfoliated flakes,[17,18,21] which are not applicable to high-volume manufacturing and large-scale memory networks.

In this work, we demonstrate 2D FeFETs using monolayer semiconducting MoS_2 and inorganic ferroelectric thin films of zirconium-doped hafnium oxide ($HfZrO_x$) with a back-gated configuration. The MoS_2 channel was synthesized through chemical vapor deposition (CVD), and the ferroelectric $HfZrO_x$ gate insulator was deposited by atomic layer deposition (ALD). Both the processes and materials are scalable and CMOS-manufacturing compatible. Our 2D FeFETs exhibit a low-voltage-driven feature ($<\pm$3 V) with hysteresis for data storage applications at room temperature, and the memory hysteresis characteristics can be further modulated by the gate bias. Moreover, the device shows synapticlike characteristics with potentiation and depression of the channel conductance when stimulated through a sequence of electric pulses. An ultrathin HfO_2 dielectric film placed between the semiconducting channel and the ferroelectric in the gate stack was found to act as a passivation layer that stabilizes the ferroelectricity of the device. Meanwhile, the device architecture of our MoS_2 FeFETs offers a noticeable amplification of the MoS_2 photoluminescence (PL), which originates from Fabry–Pérot cavity reflection of the bottom gate mirror.[22] Our results demonstrate the great potency of CVD-grown TMD/HfO_2-based ferroelectric heterostructures for future energy-efficient memory and brainlike computing applications.

The schematic structure of a back-gated single-layer MoS_2 FeFET as a nonvolatile memory cell is shown in Fig. 1(a). The process flow is depicted and described in detail in Fig. S1. A layer of Ti/Au (5 nm/70 nm) serves as the metal gate. A 15 nm thin film of $HfZrO_x$ is employed as the ferroelectric gate insulator through atomic layer deposition (ALD). The TiN layer sandwiched between the metal gate and the $HfZrO_x$ thin film effectively blocks the migrations of metal ions into the ferroelectric layer during the rapid thermal annealing (RTA) process, preventing the device from a high gate leakage current. Our devices show a low gate leakage current of $<$100 pA during operation (Fig. S2). In our study, those samples without the intermediate TiN layer suffered from significant leakage current after RTA. Next, a thin dielectric HfO_2 layer ($\sim$5 nm) was deposited on the sample to passivate the ferroelectric surface. Figure 1(b) shows the cross-sectional transmission electron microscopy (TEM) image, focusing on the gate stack of the device. The channel material, monolayer MoS_2, was first

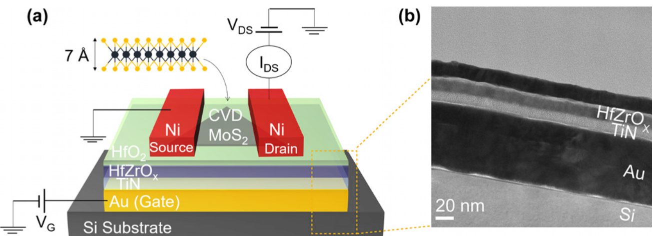

FIG. 1. (a) Schematic diagram of a single-layer MoS_2 FeFET. CVD-grown single-crystal MoS_2 is used as the transistor channel. The gate stack is composed of an Au gate electrode, TiN, $HfZrO_x$ as the ferroelectric layer, and thin HfO_2 as the passivation layer. (b) Cross-sectional view of a representative sample showing the structure and thicknesses of the gate stack. The topmost layer (dark region) is a 20 nm layer of Au coated on the sample surface for the TEM characterization.

synthesized on a SiO_2/Si substrate using our previously reported CVD method[23] and was then transferred onto the hybrid HfO_2/ferroelectric $HfZrO_x$ substrate through the wet transfer technique.

An optical image of the fabricated single-layer MoS_2 FeFET is shown in Fig. S4(a), and an AFM image focusing on the MoS_2 channel is also displayed in Fig. S4(b). A thickness of $<$1 nm evidences the monolayer nature of the MoS_2 channel used in the device. Since the underlying substrates could induce strain and charge doping in the MoS_2 crystals, we first investigate the effect of the hybrid HfO_2/$HfZrO_x$ ferroelectric substrates on the MoS_2 channel. By analyzing the shifts and broadening of phonon peaks in Raman spectra [Fig. S4(c)], we confirm that the transferred sample is slightly n-doped by the HfO_2/$HfZrO_x$ substrate,[24,25] 1% tensile strain in the as-grown MoS_2 was relaxed after the transfer process,[26] and no significantly defective crystal structure was introduced during the transfer process. More detailed discussion on Raman and PL spectra is given in the supplementary material.

The ferroelectric properties of the as-grown $HfZrO_x$ thin film were characterized through fabricating ferroelectric capacitors of Au/TiN/$HfZrO_x$/TiN/Ni with a metal/insulator/metal (MIM) structure [Fig. 2(b), insets and Fig. S8(a)]. It was found that the ferroelectric capacitor reaches a larger remnant polarization (P_r) of 48 μC/cm^2 with a coercive voltage (V_c) at $\sim$2 V when annealed at 400 °C [Fig. 2(a)]. Such a sharp polarization-voltage (P-V) hysteresis loop suggests that the leakage current through the MIM capacitors is sufficiently low.[27,28] The XRD examination reveals that the ferroelectric orthorhombic phases [o(111) and o(200)] can be substantially formed at 400 °C with suppression of the undesired monoclinic phase, and the width of the o(111) peak becomes shaper compared to 375 °C, indicating a higher crystallinity [Fig. S8(b)]. Figure 2(b) shows the capacitance-voltage (C-V) characteristic at 1 kHz of the ferroelectric capacitor annealed at 400 °C. The butterfly-shaped hysteresis curve showing the two clear polarization states is another evidence of good ferroelectricity in the as-grown $HfZrO_x$ thin film. The nonlinear response, instead of a monotonic linear curve, again manifests a low leakage current in the as-grown $HfZrO_x$. The capacitance of the ferroelectric capacitor reaches its maximum at 2.8 μF/cm^2 at $\pm$1.5 V. As a comparison, a MIM capacitor based on a dielectric HfO_2 thin film ($\sim$15 nm) shows a capacitance of $\sim$1.4 μF/cm^2, weakly depending on the applied voltages. Based on the above results, a ferroelectric $HfZrO_x$ thin film annealed at 400 °C was selected for further characterization and fabrication of our MoS_2 FeFETs.

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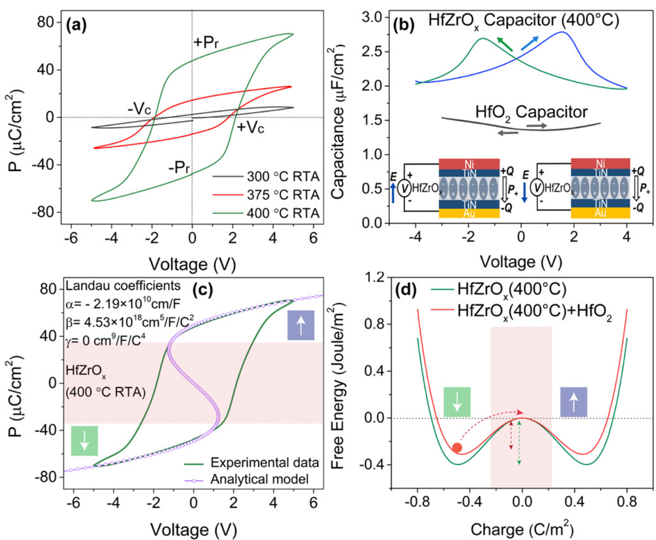

FIG. 2. (a) P-V hysteresis of the fabricated $HfZrO_x$ ferroelectric capacitors with different annealing temperatures. (b) C-V measurements of the ferroelectric capacitor annealed at 400 °C and a typical dielectric capacitor based on undoped HfO_2. Inset: schematic of polarization orientations aligned with the applied electric fields. (c) Landau coefficients extracted from (a) and the corresponding P-V characteristic plotted using the L-K model. (d) Free energy landscape of the as-grown ferroelectric $HfZrO_x$ (green curve) and the total energy of the hybrid $HfO_2/HfZrO_x$ gate stack in equilibrium.

To investigate the intrinsic properties of the as-grown $HfZrO_x$ ferroelectric, the P-V characteristic was modeled using the Landau-Khalatnikov (L-K) equation.[29] The Landau coefficients of the as-grown ferroelectric $HfZrO_x$ thin film annealed at 400 °C are extracted to be $\alpha = -2.19 \times 10^{10}$ cm/F, $\beta = 4.53 \times 10^{18}$ cm^5/F C^2, and $\gamma = 0$ cm^9/F/C [Fig. 2(c)]. In addition, Gibbs free energy of the as-grown ferroelectric $HfZrO_x$ can be further calculated based on the relationship of $V_{HfZrO_x} = dU_{HfZrO_x}/dP$ (see the supplementary material for details). Figure 2(d) plots the free energy vs charge of the $HfZrO_x$ thin film annealed at 400 °C based on the experimental Landau coefficients. The energy of the as-grown ferroelectric thin film exhibits a two-valley shape, of which the two local minima manifest that there are two stable polarization states available in the as-grown $HfZrO_x$ thin films. The region between those two valleys where $d^2U_{HfZrO_x}/dQ^2 < 0$ suggests an unstable negative capacitance state in the ferroelectric, resulting in the observed hysteresis characteristics in the $HfZrO_x$ thin films. The above results based on both experiment and simulation indicate good ferroelectricity in the as-grown $HfZrO_x$ and reinforce its candidacy of being a gate insulator for applications in FeFETs.

Next, we demonstrate back-gate FeFETs based on our CVD-grown monolayer MoS_2 integrated with the as-grown ferroelectric $HfZrO_x$ thin films. As shown in Fig. 1(a), the surface of the ferroelectric $HfZrO_x$ is passivated by a thin HfO_2 layer (~5 nm) to prevent the degradation and fluctuation of the ferroelectricity originating from trapping and detrapping centers formed at the semiconductor/ferroelectric interface.[20,30] Figure 3(d) shows the electronic transport properties (I_{DS}-V_G) of the fabricated CVD monolayer MoS_2 transistor driven by the bottom gate of the ferroelectric $HfZrO_x$ thin film. The transfer characteristics were measured at gate voltages (V_G) sweeping

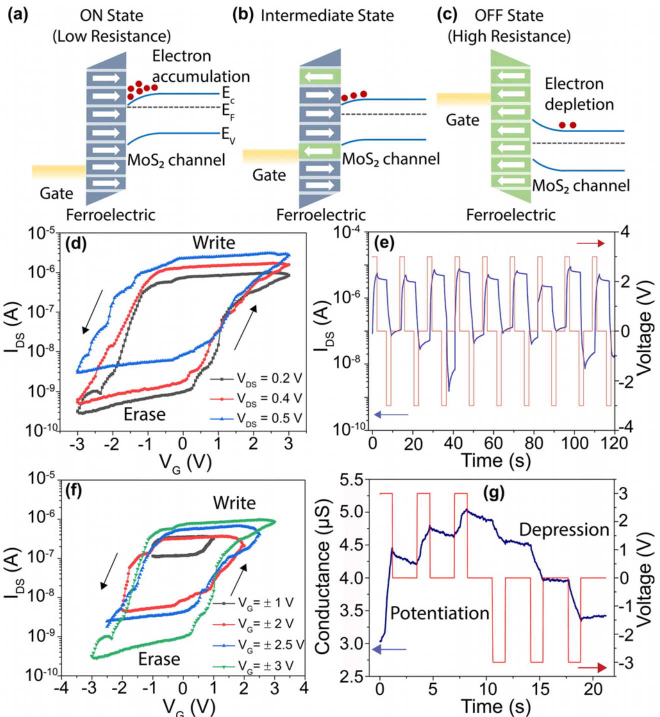

FIG. 3. (a) Energy band diagram of the MoS_2 FeFET for the basic operations, illustrating different working states including a low resistive, (b) intermediate, and (c) high resistive states. (d) I_{DS}-V_G of the MoS_2 FeFET measured at room temperature with various V_{DS}. The channel length and width of the device are 1 μm and 10 μm, respectively. (e) Current dynamics of the MoS_2 FeFET with periodic gate bias pulse ($V_{DS,\ read} = 0.4$ V). (f) I_{DS}-V_G of the MoS_2 FeFET, measured under different V_G scan ranges at $V_{DS} = 0.2$ V. (g) Sequence of pulsed voltage stimulations showing multilevel conductance states with synapticlike potentiation and depression from the MoS_2 FeFET ($V_{DS,\ read} = 0.4$ V).

between −3 V and 3 V with various drain-to-source voltages (V_{DS}). The sweeping direction is from negative to positive and then back to negative. The device shows n-type conduction with a clear counterclockwise, ferroelectric hysteresis loop, which is opposite to the transfer characteristic of a MoS_2 transistor modulated by a dielectric gate insulator (Fig. S3). The counterclockwise hysteresis suggests that the polarization switching nature of underlying ferroelectric $HfZrO_x$ is preserved in the FETs and strongly couples to the single-layer semiconducting MoS_2, giving rise to the resistive switching of the transistor channel. Specifically, during the device operation, when a positive V_G is applied, the polarization of the ferroelectric layer is directed to the MoS_2 channel, which brings the MoS_2 channel into the electron accumulation regime and results in a high drain current as the on state [or the low resistance state (LRS)], as shown in Fig. 3(a). After the V_G is removed, the $HfZrO_x$ layer remains polarized and provides a locally positive electric field on the channel. Therefore, the channel remains conductive as the LRS for the write program until the V_G becomes negative. Once a suitable negative V_G is applied, the ferroelectric polarization changes sign (pointing to the gate), which depletes the electron away from the MoS_2 channel and produces the off state, corresponding to the high resistance state (HRS) for the erase program [Fig. 3(c)].

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Such two LRS and HRS retain at $V_G = 0$ V, which signifies the desired nature of a data storage device. The on current of the MoS_2 FeFET increases as the V_{DS} increases and a large write/erase ratio of $>10^3$ between the LRS and HRS can be obtained at lower V_{DS}. Note that FeFET memory devices typically show a larger dynamic range (or on/off ratio) than that of two-terminal resistive switching devices such as phase change memory and resistive random access memory.[31] This feature of wider programmable conductance range offers FeFETs a better weight mapping capability for improving the training accuracy of the machine-learning related algorithms in which the weight range is mapped to the conductance range of the memory devices. Figure 3(e) shows the dynamic write/read/erase/read processes of the MoS_2 FeFET by applying alternating pulses onto the gate. Voltages applied to the gate of write, erase, and read were +3 V, –3, and 0 V, respectively. The dynamic write/read ratio is over 10^2 under $V_{DS} = 0.4$ V. From the transfer characteristic, we note that the MoS_2 FeFET shows as a higher off current of 10^{-9} A than that of our typical CVD MoS_2 transistor using a SiO_2 dielectric gate stack, suggesting a higher degree of electron doping level in the channel of the MoS_2 FeFET. This can be attributed to the charge transfer between the CVD MoS_2 and the HfO_2 passivation layer that leads to n-type doping of the MoS_2 channel, as observed from the Raman and PL spectra shown in Figs. S4(c) and S4(d). Further improvement in the on/off current ratio of the MoS_2 FeFETs should be able to achieve through reducing the charge transfer at the MoS_2/HfO_2 surface, for example, by introducing a few layers of chemically inert 2D hexagonal boron nitride (hBN) that physically separate the MoS_2 channel and HfO_2.

On the other hand, compared to other 2D FeFETs reported in previous studies, we note that our MoS_2 FeFET can reach one order of magnitude higher current at the LRS with a much smaller driving voltage (±3 V), indicating a more efficient gate control in our device. For example, the 2D FeFETs using ferroelectric P(VDF-TrFE) and 2D $CuInP_2S_6$ show an on current of $\sim 10^{-7}$ A with switching voltages of ±40 V and ±5 V, respectively.[17,18] The ferroelectric hysteresis loop in the I_{DS}-V_G characteristics of the MoS_2 FeFET can be further modulated by applying different gate biases [Fig. 3(f)]. With a larger V_G, a larger hysteresis loop can be obtained, illustrating the on/off current ratio of the MoS_2 FeFET is controllable through adjusting the gate bias. A clear ferroelectric hysteresis characteristic with two distinct states can maintain even at a smaller V_G range, although the corresponding on/off ratio decreases. It is likely that the thin HfO_2 layer inserted between the semiconducting MoS_2 channel and the ferroelectric $HfZrO_x$ layer plays two crucial roles: (i) preserving the ferroelectricity of the underlying $HfZrO_x$ through surface passivation and (ii) lowering the threshold switching voltage of the device. First, it was reported that in the organic FeFETs, there exists polarization fluctuation at the semiconductor/ferroelectric interface.[30] Such polarization fluctuation can be suppressed by placing a thin buffer layer of PMMA between the channel and ferroelectric insulator, thus improving the device performance. Accordingly, the thin layer of HfO_2 in our device could act as a buffer layer that suppresses the polarization fluctuation and retains the ferroelectricity. Second, since the thin dielectric HfO_2 layer exhibits a finite capacitance with a free energy of $U_{HfO_2} = Q^2/2C_{HfO_2}$ (Fig. S6), when connected in series to the ferroelectric layer, the energy of the hybrid $HfO_2/HfZrO_x$ gate stack can be redistributed to U_{gate} $(= U_{HfZrO_x} + U_{HfO_2})$.[32] Figure 2(d) illustrates the total energy of the hybrid $HfO_2/HfZrO_x$ gate stack based on the experimentally extracted Landau coefficients and the measured capacitance. It can be seen that the presence of the thin HfO_2 passivation layer in the gate stack effectively lowers the energy barrier between the two polarization states in the ferroelectric, which is fundamentally associated with the threshold of the switching voltage for a ferroelectric-based device. Therefore, the ferroelectric characteristic in FeFETs is able to appear when a sufficient gate bias is applied. As can be seen in Fig. S7, a MoS_2 FeFET without the thin HfO_2 passivation layer shows no ferroelectric characteristics at the same range of gate bias, indicating the significance of the presence of the thin HfO_2 passivation layer in the device. Table S1 summarizes the key parameters of the reported FeFETs using different ferroelectrics and channel materials. Among these devices, the FeFET based on the CVD $MoS_2/HfZrO_x$ heterostructure shows the feature of low-power consumption. Finally, we demonstrate the synaptic-like behavior from our MoS_2 FeFET. Figure 3(g) displays the dynamic response of the MoS_2 FeFET-based synapse by applying sequences of pulsed voltage stimulations with identical amplitudes, durations, and intervals, and the change in channel conductance was simultaneously monitored. The conductance of the device increases and decreases with the sequential electrical excitations in a stairlike way, thus producing multilevel conductance states. Such programmable and cumulative conductance fundamentally benefits from the nature of multidomain switching dynamics in the ferroelectric $HfZrO_x$ gate oxide [Fig. 3(b)]. The fraction of the ferroelectric polarization charge in the certain orientation can be increasing with the sequential pulsed stimulations. Then, the changes in the net polarization charge modulate the transistor threshold voltage, and therefore, the channel conductance (at a fixed gate read voltage). The observed potentiation and depression of the conductance dynamics and the low-voltage-driven characteristic of the CVD MoS_2 FeFETs promises future applications in electronic synapses for artificial neural networks (i.e., machine/deep learning).[33,34] Our results have provided preliminary but important insights into the design and integration of synthetic TMDs and HfO_2-based ferroelectrics for energy-efficient 2D memory devices.

In summary, 2D FeFETs using CVD-grown monolayer MoS_2 and a hybrid $HfO_2/HfZrO_x$ ferroelectric gate insulator have been demonstrated. The devices show memory hysteresis characteristics and feature a low operating voltage, a good on/off ratio, multilevel conductance states, and an insignificant leakage current at room temperature. The ferroelectric characteristics of the devices can be further modulated by the gate biases. The thin HfO_2 layer in the gate stack effectively passivates the ferroelectric surface to stabilize the device operation and enables lower switching voltages though the energy redistribution of the gate stack. The 2D FeFETs exhibit programmable, cumulative conductance for electronic synapse applications. Based on our FeFETs structure, the integration of synthetic 2D semiconducting TMDs and inorganic HfO_2-based ferroelectrics shows great promise for future applications in large-scale high-performance nonvolatile memory and neuromorphic computing systems.

See the supplementary material for Figs. S1–S8, CVD and transfer processes of MoS_2, process flow of the device fabrication, discussion on the MoS_2 Raman and PL characterization, and method for the Gibbs free energy calculation.

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