MITSUBISHI ELECTRIC RESEARCH LABORATORIES
https://www.merl.com

# Recent Development in 2D and 3D GaN devices for RF and Power Electronics Applications

Teo, Koon Hoo; Chowdhury, Nadim; Zhang, Yuhao; Palacios, Tomas; Yamanaka, Koji; Yamaguchi, Yutaro

TR2020-162 December 16, 2020

**Abstract**

Some recent developments in 2D and 3D GaN devices and their improved performance parameters such as efficiency, fT, linearity, power density and switching speed are briefly outlined. Most of the cases briefed are for applications in RF with one example for power electronics and another for GaN integrated circuit.

*IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*



Mitsubishi Electric Research Laboratories, Inc.
201 Broadway, Cambridge, Massachusetts 02139

# Recent Development in 2D and 3D GaN devices for RF and Power Electronics Applications


Koon Hoo Teo
Multi-Physics and Dynamic Group
Mitsubishi Electric Research Labs
Cambridge, MA, USA
teo@merl.com

Nadim Chowdhury
Dept of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, MA, USA
nadim@mit.edu

Yuhao Zhang
Center for Power Electronics Systems)
Virginia Polytechnic Institute and State University
Blacksburg, VA, USA
yhzhang@vt.edu

Tomas Palacios
Dept of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, MA, USA
tomasp@mit.edu

Koji Yamanaka
Information Technology R&D Center
Mitsubishi Electric Corporation
Kamakura, Kanagawa,Japan
Yamanaka.Koji@cj.MitsubishiElectric.co.jp

Yutaro Yamaguchi
Information Technology R&D Center
Mitsubishi Electric Corporation
Kamakura, Kanagawa,Japan
Yamaguchi.Yutaro@cj.MitsubishiElectric.co.jp



***Abstract*— Some recent developments in 2D and 3D GaN devices and their improved performance parameters such as efficiency, fT, linearity, power density and switching speed are briefly outlined. Most of the cases briefed are for applications in RF with one example for power electronics and another for GaN integrated circuit.**



***Keywords—GaN, Semiconductor Devices, Integrated Circuits, 2D and 3D Semiconductor Devices, RF, Power Electronics***


## I. INTRODUCTION

GaN devices has been accepted as a technology which shows many merits for applications in RF [1] and power electronics[2]. There are many variations in the device design since its introduction, ranging from the use of different materials to device design architecture. For RF applications, especially in RF power amplifier, the focus of the device design has been on power density, $f_T$, efficiency, linearity and gate threshold voltage. Similarly, for the application in power electronics, enhancement mode, power density, efficiency and switching speed are some of the parameters researchers paid great attentions. This paper will focus on some of the recent 2D and 3D device designs, which include lateral and vertical structures to 3D design such as GaN FinFET, p-type and n-type GaN, Ga and N polar devices, that help to improve the values of those parameters that improve the performance of device for applications in RF and power electronics, including control circuitries.

.

## II. 2D GAN DEVICES

HEMT (high electron mobility transistor) is among the first 2D GaN device designs to be used for RF applications. Since then, there are many variation of the design that includes the use of multi-channel GaN, N-polar GaN, diamond backbarrier, p-type gate, P-type channel GaN and etc.

Fig 1(a) and (b) show an N-polar $Al_{0.8}Ga_{0.2}N$/AlN with a continuously graded channel Pol-FET on SiC and its input/output performance [3]. Transistors with a source to drain distance of 12 $\mu$m had a maximum drain current of 62.8 mA/mm for gate voltage of +4 V and an on/off current-ratio of $1.1 \times 10^4$. The maximum drain current was stable between 20 C and 250 C operating temperatures. With the addition of 30-nm-thick $Al_2O_3$ gate insulator the maximum drain current increased to 126 mA/mm. This is the highest value reported for an AlGaN/AlN heterostructure so far.

Fig 2 (a) show a InAlN/GaN high electron mobility transistors (HEMTs) with 40–200 nm rectangular gates and 300–700 nm source-to-drain distances were fabricated on Si substrates [4]. The device with 40-nm gate and 300-nm source-to-drain distance exhibited a high drain current of 2.66 A/mm (a transconductance (gm) of 438mS/mm, and a high current gain cutoff frequency ($f_T$) of 250 GHz. To the best of our knowledge, this is the highest f T value reported so far for GaN-based transistors on Si.

Fig. 3 (a) shows the device schematic and SEM image of the $V_T$-engineered -fin device, with fins of varying width present within the 250 nm length gate region, while the access regions remain planar [5]. Fig. 3(b) shows the transfer characteristics of 250 nm LG for a standard planar (blue), type-II M- fin (black) and type-I M-fin (red) devices. The device current for the same gate overdrive (VG-VT) is lower for the type-I device, due to its higher access resistance, whereas the device current for the type-II device is equivalent to the planar device. Fig. 3(c)-(e) show the gm, g′m and g″m respectively for the three

devices. It can be seen that the $g_m$ (Fig. 3(c)) of the type-I M-fin and planar devices degrades after the device turns on, due to access-region depletion (or also called 'source-starvation effect'). The $g_m$ for the type-I M-fin device is also lower than the planar device due to the higher access region resistance caused by the fin-structures. The $g_m$ for the type-II M-fin device on the other hand displays nearly flat behavior after the device turns on, and is comparable in magnitude to the peak $g_m$ of the planar device because of the wider effective width of access regions. Simultaneously, the $g_m$ for this device also has a gentler off-to-on transition slope, similar to the type-I M-fin device, due to the $V_T$ engineering described earlier. The lower $g'_m$ and $g''_m$ for both M-fin devices as compared to the planar device can be seen in Fig. 3(d)-(e), with type-II device showing least derivatives in the full $V_G$-regime. Figs. 3(f) and (g) show the small signal ($h_{21}$) and unilateral gain ($U_{max}$) as a function of frequency for the three devices. The cutoff frequencies $f_T$ and $f_{max}$ are in the range of 26-46 GHz and 50-60 GHz respectively, for all the devices.

Fig. 4 (a) shows the schematic image of negative capacitance gated AlGaN/GaN HEMT [6]. The utilization of negative capacitance as the gate dielectric yields a voltage amplification at the gate leading to an amplification of transconductance as shown in Fig. 4 (b). A thicker $HfZrO_x$ yields a higher amplification and vice versa.

Fig 5 (a) show the use of p-diamond back-barriers (BBs) and cap layers to enhance the performance of GaN-based high electron mobility transistors (HEMTs) [7]. Diamond can offer a heavily doped p-type layer, which is complementary to GaN electronics. Two sets of source-to-gate distance ($L_{sg}$), gate length ($L_g$), and gate-to-drain distance ($L_{gd}$) are selected to simulate power and microwave devices. Self-consistent electrothermal simulations reveal that the use of p-diamond BBs and cap layers can increase the breakdown voltage of GaN-based HEMTs by fourfold, at the same time that they enhance the 2-D-electron-gas confinement and reduce short channel effects. These results highlight that p-diamond layers can improve the performance of GaN HEMTs for high-power and high-frequency applications beyond the thermal improvements pursued until now.

## III. 3D GaN Devices

Fig 6 shows the architecture of a novel vertical GaN device. This device presents the first experimental study on capacitances, charges, and power-switching figure of merits (FOM) for a large-area vertical GaN power transistor [8]. A 1.2-kV, 5-A GaN vertical power FinFET was demonstrated in a chip area of 0.45 mm2, with a specific on-resistance of 2.1 mohm cm2 and a threshold voltage of 1.3 V. Device junction capacitances were characterized and their main components were identified. This was used to calculate the switching charges and practical switching frequencies. Device FOMs were then derived that take into account the trade-offs between the conduction and switching power losses. The GaN vertical FinFETs exhibit high-frequency (MHz) switching capabilities and superior switching FOMs when compared with commercial 0.9-1.2-kV Si and SiC power transistors. This shows the great potential of GaN vertical FinFETs for next generation medium-voltage power electronics.

## IV. GaN Intergrated Circuits

Fig 7 demonstrates a complementary logic circuit (an inverter) on a GaN-on-Si platform without the use of regrowth technology. Both n-channel and p-channel GaN transistors are monolithically integrated on a GaN/AlGaN/GaN double heterostructure [9]. N-channel FETs show enhancement-mode (E-mode) operation with a threshold voltage around 0.2 V, ON-OFF current ratio of 107 and $R_{ON}$ of 6 Ω·mm, while the p-channel FETs show E-mode operation with Vth of −1 V, ON-OFF current ratio of 104 and $R_{ON}$ of 2.3 kΩ·mm. Complementary logic inverters fabricated with this technology yield a record maximum voltage gain of ~ 27 V/V at an input voltage of 0.59 V with $V_{DD}$=5 V.

## V. Conclusions

This paper presented an outlined report on some of the latest development in 2D and 3D GaN devices with improved parameter values in linearity, efficiency, power density, switching speed and the realization of GaN CMOS and a demonstration of the feasibility of a GaN integrated circuit.

## References


[1] F Zeng, Judy X An, G Zhou, W Li, H Wang, T Duan, L Jiang and H Yu, A Comprehensive Review of Recent Progress on GaN High Electron Mobility Transistors: Devices, Fabrication and Reliability, Electronics 2018, issue 7, Vol 377

[2] H Amano1, Y Baines, E Beam, Matteo Borga , T Bouchet, Paul R Chalker, et al, The 2018 GaN power electronics roadmap, J. Phys. D: Appl. Phys. 51 163001, 2018

[3] J. Lemettinen, N. Chowdhury, H. Okumura, I. Kim, S. Suihkonen and T. Palacios, "Nitrogen-Polar Polarization-Doped Field-Effect Transistor Based on Al0.8Ga0.2N/AlN on SiC With Drain Current Over 100 mA/mm," in IEEE Electron Device Letters, vol. 40, no. 8, pp. 1245-1248, Aug. 2019.

[4] W. Xing et al., "InAlN/GaN HEMTs on Si With High $f_T$ of 250 GHz," in IEEE Electron Device Letters, vol. 39, no. 1, pp. 75-78, Jan. 2018.

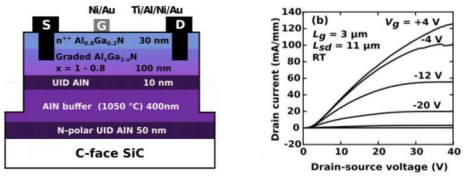
[5] S. Joglekar, U. Radhakrishna, D. Piedra, D. Antoniadis and T. Palacios, "Large signal linearity enhancement of AlGaN/GaN high electron mobility transistors by device-level Vt engineering for transconductance compensation," 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, 2017, pp. 25.3.1-25.3.4.

[6] Koon Hoo Teo, N. Chowdhury "High electron mobility transistor with negative capacitor gate" US10276704B1, 2017

[7] Y. Zhang, K. H. Teo and T. Palacios, "Beyond Thermal Management: Incorporating p-Diamond Back-Barriers and Cap Layers Into AlGaN/GaN HEMTs," in IEEE Transactions on Electron Devices, vol. 63, no. 6, pp. 2340-2345, June 2016.

[8] Y. Zhang, J Perozek, Z Liu, A. Zubair, D. Piedra, N. Chwdhury, X. Gao, K Shepard, T. Palacios, "Large Areas 1.2-kV GaN Vertil Power FinFET with a Record Switcing Figure of Merit," in IEEE Electron Device Letters, vol. 40, no. 1, Jan 2019

[9] N. Chowdhury, Q. Xie, M. Yuan, K. Cheng, H. W. Then, and T. Palacios, "Regrowth-free GaN-based complementary logic on a Si substrate," IEEE Electron Device Letters vol. 41, 2020 (DOI: 10.1109/LED.2020.2987003)




(a) (b)

Fig 1:(a) Schematic cross-section of the fabricated N-polar AlGaN/AlN PolFET with recessed source/drain contacts. (b) N-polar PolFET with a 30-nm-thick $Al_2O_3$ gate insulator DC output characteristics for gate-source voltage from +4 V to −36 V.

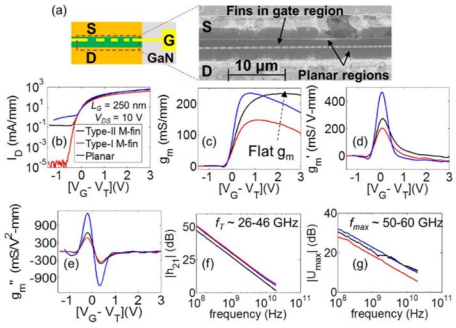
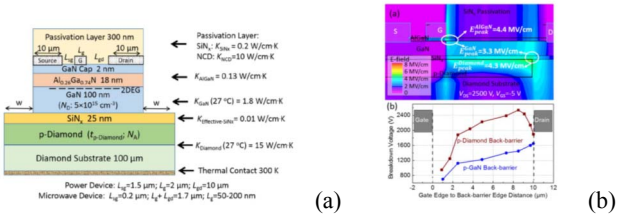



Fig 3: (a) Schematic and SEM image of $V_T$-engineered-fin device. (b) ID-VGS transfer curves for type II M-fin (black), type-I M-fin (red) and regular planar (blue) devices. (c) gm vs. VGS curves for the devices in (b).(d) g′m vs. VGS. and (e) g″m. vs. VGS for the devices in (b) reduced gm derivatives in the M-fin devices as compared to the planar device. (f) Current-gain (h21) and (g) Unilateral gain (Umax) for the devices in (b). The cutoff frequencies fT and fmax are in the range of 26-46 GHz and 50-60 GHz respectively, for all the devices.




(a) (b)

Fig 5 **:**(a) GaN-on-diamond HEMTs with a p-diamond BB with thermal conductivity of different layers and thermal contact settings. (b) Simulated electric field distribution in GaN-on-diamond HEMTs with a patterned p-diamond BB, at the bias of $V_{GS}$ = −5 V and $V_{DS}$ = 2500 V. Gate edge to BB edge distance is 8.5 $\mu$m. (c) Dependence of device BV on the gate edge to BB edge distance for GaN HEMTs with p-diamond and p-GaN BBs.

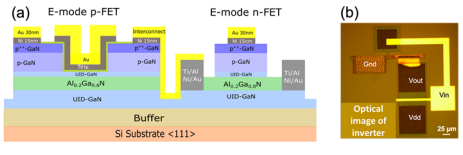
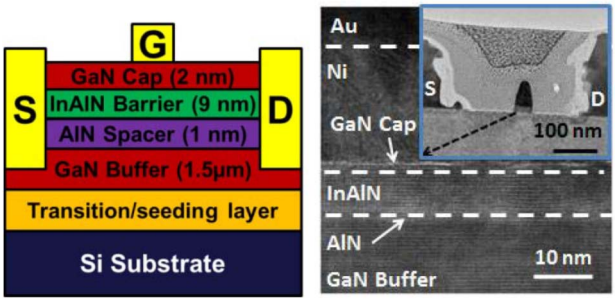
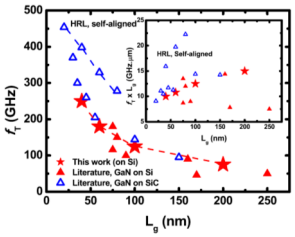



Fig 7: (a) Schematic of the demonstrated GaN complementary circuit platform; (b) Optical image of the complementary logic inverter fabricated on this platform.

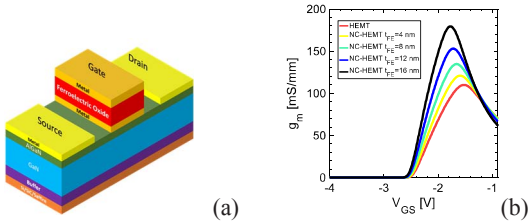



(a)




(b)

Fig 2: (a) Schematic diagram and TEM image (gate region) of a 40-nm gate InAlN/GaN on Si (b) Output Characteristics (c) Comparison of the cut-off frequencies ($f_T$) of GaN HEMTs on Si in this work with other reported GaN HEMTs on Si. The inset shows the $L_g$ dependence of $f_T$ .Lg product.




(a) (b)

Fig 4: (a) Schematic of a negative capacitance ($HfZrO_x$) gated AlGaN/GaN HEMT (b) $g_m$-$V_{GS}$ characteristics for different ferroelectric oxide thickness of the NC-gated HEMT.

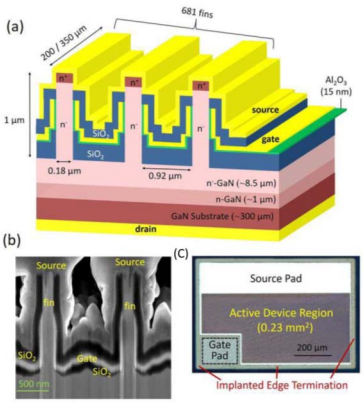



Fig 6: Schematics of the GaN vertical power FinFETs with multiple fin channels. (b) Cross-sectional SEM image of the fin area in the fabricated device, taken in a focused ion beam system. (c) Optical microscopy image of the fabricated large-area device