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International Conference on Electron Device Meeting Report

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Abstract

This report summarizes the progress made in Gallium Nitride (GaN) and some other semiconductor device technology as reported at the 66th International Electron Devices Meeting which was held for the first time via solely on on-line video conference from Dec 12 to 18, 2020. This year conference covers many topics which includes, as usual GaN devices for RF and Power Electronics applications, diamond devices, switches using ferro-electric technology, quantum computing, hardware accelerators for neuron networks, etc.

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Executive Summary

The 66th International Electron Devices Meeting was held for the first time via solely on on-line video conference from Dec 12 to 18, 2020. This year conference covers many topics which includes, as usual GaN devices for RF and Power Electronics applications, diamond devices, switches using ferroelectric technology, quantum computing, hardware accelerators for neuron networks, etc.

There were a few papers reporting on using ferroelectric material designed for switches. The basic physics is to utilize the switching mechanism during the reversal of their polarizations. This technology is being explored to be used as 3D memory technology and supposed to consume much lower energy than the conventional CMOS technology.

There are quite a number of papers on GaN technology and could be classified into p-type GaN, multi-channel GaN, GaN integration technology and integration with Si technology, higher frequency for GaN lateral devices, GaN devices as a fast switch for applications particularly in motor and motor drive applications, vertical structure GaN devices for power electronics. For GaN technology in RF applications, the focus was on p-channel, integration technology, power density and increasing frequency.

P-type GaN: two enhancement mode designs were reported. Firstly, the device has shown experimentally to provide an enhancement-mode with threshold voltage of −0.5V. In another report, using an added circuit topology, E-mode p-GaN gate HEMTs achieving a threshold voltage of +3.6 V to +8.2 V been demonstrated on the commercial GaN-on-Si platform. In another paper, it was reported that GaN/AlN p-channel HFET could achieve Imax of 420 mA/mm and a unity gain frequency of fT of 20GH. These were achieved by exploiting the high-density polarization-induced 2D hole gas of the GaN/AlN heterostructure, best ohmic contact, and proper scaled T-gate design.

One report also showed that HEMT epitaxy and processing on Si substrate have significantly impact on the RF losses and linearity. Another reported the use of a 19nm gate with proper InGaAs composition HEMT to achieve a fT of 738GHz and fmax of 492 GzHz.

For vertical GaN, among the paper of interest is a report on the design of a high voltage GaN P=N diode. A reverse breakdown voltage of 4.16 kV (defined at 1 µA reverse current) is achieved.

GaN for power electronics and power IC: GaN power IC's is the next frontier where it could release the full potential of GaN power electronics. Gallium Nitride power integrated circuits are demonstrating unparalleled efficiency, density, and system cost competitiveness. An integrated gate driver is demonstrated with enhanced performance, in which a bootstrap circuit is utilized to achieve high output voltage with fast switching speed. Future opportunities may in multi-functional devices, including the combination of CMOS technology and GaN/SiC hybrid power IC's to provide optimum performance.

GaN and Si integration: Comparison was made on different approaches to the research in GaN and Si CMOS integration, including utilizing 3D monolithic layer transfer to achieve the best of GaN and Si CMOS technologies on a single wafer.

Switching GaN: a 1.2-kVclass, 4-A normally-off vertical GaN using fin-channel JFET on a GaN substrate has been demonstrated. The device is capable of achieving an on/off current ratio of ~10^9 , a threshold voltage of more than 0.5 V with a drain current of 1 mA and an on-resistance of 0.82 mΩ·cm^2. In another paper, GaN power transistors has demonstrated a great reduction in power loss with respect to IGBT or MOSFET-based inverters. However, the challenge remains the controlling switching speed (dv/dt)..

For SiC technology: A medium-scale integration ICs fabricated by NASA Glenn Research Center has shown to successfully operate for over a period of 1 year in 500 °C air-ambient, for 60 days in 460 °C and under 9.3 MPa pressure, in temperature cycle of -190 °C to +812 °C, and exposed to radiation at 7 MRad(Si) ionizing dose and 86 MeV-cm2 /mg heavy ion strikes.

For Si technology, a 40kV Si Vacuum transistor was reported. Electrons are released from into vacuum through tunneling, moving through vacuum and being collected at the anode. As a result, it is the vacuum that determines the properties of transport and the high voltage isolation of the device. The capacitance of the terminals is about 50 aF/tip, which implies that the fT would have a ceiling between 1-10 GHz.

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